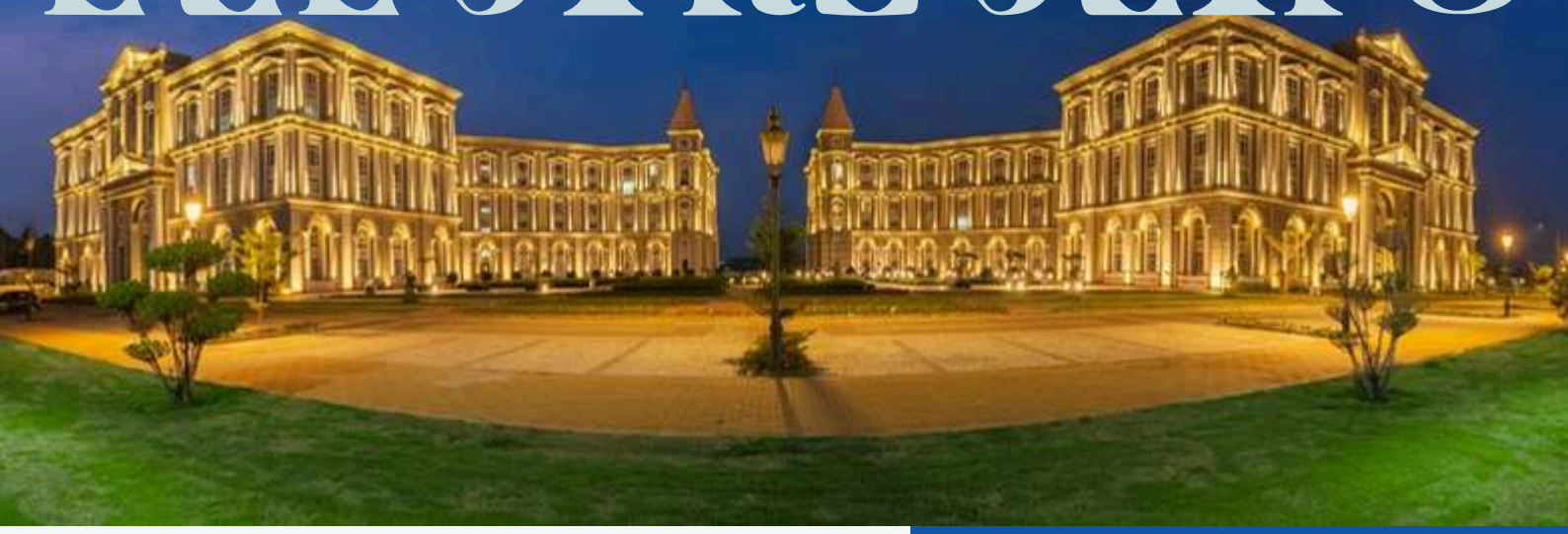
DAYANANDA SAGAR UNIVERSITY

JANUARU-JUNE 2026
VOLUME 6 | ISSUE 1 | 2026

ELECTROCAPS



Main Campus

Dayananda Sagar University

SCHOOL OF ENGINEERING

DEVARAKAGGALAHALLI, HAROHALLI,
KANAKAPURA ROAD, RAMANAGARA - DISTRICT,
KARNATAKA - 562112

Volume 6 Issue 1
Presented by
Electroblitz Club

Department of Electronics & Communications Engineering





ABOUT THE DEPARTMENT

Dayananda Sagar University, School of Engineering started with the Electronics and Communication Engineering (ECE) Department in the year 2015. As a unit of excellence, the Department is well committed to impart the knowledge with highly qualified and well specialized faculty in the vistas of Electronics and Communication. The department has well established infrastructure and innovative labs put in place to facilitate the first and experience to students, for its academic and research programs. It runs four programs namely UG, PG with specialization of Embedded systems, B.Voc in Mechatronics and Doctoral degree. The department has collaborated with NTTF to offer the Vocational degree. This program enables the graduating students to accept a professional career which demands very high-level industry relevant skills. An exclusive BOSCH REXROTH lab is integrated into the curriculum and students can conduct automation projects. The industry sponsored Analog Devices Lab also provides students with opportunities to conduct research in the Communication Domain. The department faculty have patents and sponsored research projects funded by various Government funding agencies.

VISION

"To create innovative Engineers and Entrepreneurs with technological excellence, professional commitment and social responsibility for serving national and global needs. "

MISSION

Inculcate Academic Excellence through innovative teaching and learning processes and espousing appropriate pedagogical parameters.

Reinforce the Students with desired technical aptitude, entrepreneurial and leadership skill sets enabling them to face the challenges of globalization and technological sophistication.

Initiation with understanding the psychology of students, socio-cultural aspects of the bidirectional learners, vitality of interdisciplinary approach, value addition through interactive and collaborative learning. This is followed by systematic and sequential implementation of syllabus upgradations on par with industrial revolution.



Program Educational Objectives (PEOs) - UG

Our Graduates will have in-depth knowledge of Electronics and Communication Engineering with promising professional careers in private and public sector or higher education.

Our Graduates will have the motivation for perennial learning and progress their careers by inculcating interpersonal, leadership and social skills.

Our Graduates will be successful in solving Engineering Problems with innovative ideas and acquire managerial skills for desired outcomes.

Our Graduates will be active members for catering to the society locally and globally with Ethics and Integrity.

Program Educational Objectives (PEOs) - PG

Analyze and formulate suitable Electronic Design Automation (EDA) to solve real world problems in the Embedded Systems domain to design innovative products and systems

Develop managerial skills and relevant techniques in the disciplines of Embedded Systems that include safety and sustainability, and become a successful professional or entrepreneur in the sector.

Pursue a career in Embedded Systems research by selfteaching and selfdirected research on cutting-edge technology

Program Educational Objectives (PEOs) - B.Voc

Our Graduates will have in-depth knowledge of Mechatronics (B.VoC) with promising professional careers in private and public sector or higher education.

Our Graduates will be successful in solving Engineering Problems with innovative ideas and acquire managerial skills for desired outcomes.

Our Graduates will have the motivation for perennial learning and progress their careers by inculcating interpersonal, leadership and social skills.



Program Specific Outcome (PSO) - UG

Apply the knowledge of Electronics and Communication to solve Engineering Problems in various domains of Engineering Sciences.

Adopting analytical skills and complementing the cross-cutting technology to arrive at optimum solutions for Engineering Problems.

Adaptability to dynamic work environment to address the societal needs with ethical approach.

Program Specific Outcome (PSO) - PG

Develop skills in Embedded Systems, Design, Testing, Verification, and prototyping with a focus on applications.

Integrate numerous subsystems to create a System On Chip, enhance its performance, and excel in Embedded domain-related industries

Apply use contemporary design tools for efficient product development.

Program Specific Outcome (PSO) - B.Voc

Apply the knowledge of Mechatronics to solve Engineering Problems in various domains of Engineering Sciences.

Adopting analytical skills and complementing the cross-cutting technology to arrive at optimum solutions for Engineering Problems.

Adaptability to dynamic work environment to address the societal needs with ethical approach.

DEAN'S DESK



Dr. Udaya Kumar Reddy K R

I am delighted that the Department of Electronics and Communication Engineering is bringing out the magazine that can provide wonderful insights for students and faculty fraternity. A lot has been happening in Electronics Sciences over the years, and one of the significant changes involves this newsletter. Our graduate students are doing amazing things in many different areas in different ways . In the current issue, you 'll meet some remarkable students and faculty who are making a difference in the technical aspects and otherwise. we are hoping to build this endowment with your support, to afford even more opportunities for students to take part in this important component of their graduate education, I hope this magazine provides the reader a wonderful insight and i thank the editorial team for their wonderful effort in bringing out this masterpiece.

WISH YOU ALL THE BEST.

CHAIRMAN'S DESK



Dr. Arun Balodi

Dear All, I hope this message finds you well and in good spirits. As we embark on another exciting year filled with opportunities and challenges, I wanted to take a moment to connect with each one of you. The Electronics and Communication Engineering Department has always been a vibrant community of passionate individuals dedicated to advancing knowledge, pushing boundaries, and contributing to the ever-evolving field of Electronics and Communication Engineering. Our collective efforts have resulted in numerous achievements, accolades, and a reputation for excellence. Firstly, I would like to express my gratitude to our dedicated faculty, passionate students, and supportive staff for their continued commitment to excellence in teaching, research, and innovation. Your collective efforts have positioned our department as a leader in advancing cutting-edge technologies and shaping the future of Electronics and Communication Engineering.In the spirit of fostering a sense of community and celebrating our achievements, I am pleased to announce the upcoming release of the Electronics and Communication Engineering Department Magazine. This publication aims to showcase the remarkable work, accomplishments, and stories within our department. I encourage you all to actively engage in departmental activities, research initiatives, and various events that will be organized throughout the year. Your unique perspectives and skills contribute significantly to the dynamic and enriching environment that defines our department T Your dedication and passion are the driving forces behind our success. I am confident that, together, we will continue to excel and make lasting contributions to the world of Electronics and Communication Engineering. “The focus of the department is to provide a better campus-based educational experience to the students for developing their learning interest and critical thinking to increase competencies in them. "

EDITORIAL MESSAGE

Spark Ignition: The Unwritten Code of Our Community

Dear ECE family, As we navigate the ever-changing landscape of technology and innovation, it's easy to get lost in the noise. But amidst the hum of circuit boards and the glow of succes, there's a thread that weaves us together, our passions for electronics.

Electroclips is more than just a magazine; it's a spark plug for our community. It's where stories meet innovation, where dreams become reality, and where friendships are forged. Every issue is a snapshot of what makes us tick, a testament to the diversity of talents, perspectives, and backgrounds that make ECE so vibrant.

We're not just talking about achievements; we're talking about experiences. We're talking about late-night hackathons, project triumphs, and failures turned into lessons learned. We're talking about students who've dared to dream big, staff who've mentored with heart, and alumni who have paved the way for those who come next.

This magazine is a time capsule of our collective spirit – one that's fueled by curiosity, creativity, and a willingness to learn. By contributing your stories, ideas, and talents to Electroclips, you're not just writing history; you're creating it.

So, let's spark some ignition in our community! Let's share our passions, showcase our work, and celebrate each other's successes. Together, we can create something truly remarkable – a magazine that embodies the essence of ECE and inspires others to join us on this incredible journey.

Join us on this spark-filled adventure!

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DAYANANDA SAGAR UNIVERSITY

Dayananda Sagar University (DSU) is a premier private university located in Bangalore, India, dedicated to fostering excellence in education, research, and innovation. Established under the Dayananda Sagar Institutions (DSI) legacy, DSU continues to uphold a tradition of academic excellence and industry-oriented learning.

Department of Electronics and Communication Engineering

The Electronics and Communication Engineering department of at Dayananda Sagar University, established in 2015, offers UG, PG, B.Voc, and Doctoral programs. Key specialization areas include Embedded Systems, VLSI, and Wireless Sensor Networks. Supported by collaborations with NTTF, BOSCH REXROTH, and Analog Devices, students gain strong hands-on and research exposure, while faculty actively contribute through patents and government-funded projects.

Department of Aerospace Engineering

The Aerospace Engineering Department at Dayananda Sagar University, established in 2018, offers a B.Tech program with advanced labs and a Centre of Excellence in collaboration with Dassault Systems. The curriculum provides strong industry exposure, preparing students for careers in design, aerodynamics, propulsion, and avionics. Students gain hands-on experience through projects, simulations, and research under experienced faculty.

Department of Data Science Engineering

The Data Science Engineering program at Dayananda Sagar University focuses on building strong foundations in data analysis, machine learning, and artificial intelligence. It equips students with practical skills to extract insights from data and solve real-world problems across various domains.

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Dr. Udaya Kumar Reddy K. R, Dean - SoE, DSU

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Dr. Nagaraja S.R, Chairperson, ASE, DSU
Dr. Shaila S.G, Chairperson, CSE(Data Science), DSU

ORGANISERS
Dr. Divyashree H.B, Assistant Professor, ECE, DSU
Dr. Prashantha Kumar H.G, Associate Professor, ASE, DSU
Prof. Shivamma D, Assistant Professor, DS, DSU

ABOUT THE EVENT

CELESTAI' is a premier national-level technical fest hosted at Dayananda Sagar University, bringing together innovation and creativity on a dynamic platform. The event features exciting competitions such as Robosoccer, Skyrift, and Hack Hustle, along with various technical events.
Participants engage in hands-on challenges across domains like robotics, coding, AI, and emerging technologies. The fest encourages problem-solving, teamwork, and real-world application of technical skills. CELESTAI' provides a collaborative environment where students can innovate, compete, and showcase their talents.
It also offers opportunities to interact with peers and gain exposure at a national level.

INDIA'S AI-FIRST UNIVERSITY

DAYANANDA SAGAR UNIVERSITY

Presents

CELESTAI

DSU TECHFEST CELESTAI

23rd - 25th April 2026

ORGANISED BY

Department of Electronics and Communication Engineering, Department of Aerospace Engineering & Department of Data Science Engineering

EVENTS TRACKS

RoboSphere (Robotics & Automation) :
Focused on intelligent machines and robotic innovations, this track includes events like Robosoccer and other automation challenges. Participants explore robot design, control systems, and real-time problem-solving in dynamic environments.

AeroVision (Aerial & Drone Tech) :
Dedicated to aerospace and drone-based challenges such as Skyrift, this track emphasizes UAV design, flight control, and aerial innovation. Teams work on building efficient flying systems and tackling real-world aerial tasks.

Hack Hustle (Hackathon & Coding) :
A fast-paced innovation track where participants solve real-world problems through coding and development. It includes hackathons focused on AI, web/app development, and creative software solutions under time constraints.

Techzibition (Project Expo & Innovation Showcase) :
A platform for participants to present innovative projects, prototypes, and research ideas across various domains of technology. .

GAME RUSH (Gaming & Esports Arena) :
A fast-paced gaming track featuring competitive esports and interactive challenges. Participants showcase their skills, strategy, and teamwork in an exciting and engaging environment.

TECHQUEST (Technical Treasure Hunt) :
A knowledge-driven track testing participants on core technical concepts, problem-solving, and current trends through engaging quiz-based competitions.

Posterverse (Poster Presentation & Design) :
A creative track where participants present ideas through impactful posters, combining visual design with clear technical or conceptual communication.

CHIEF GUEST

Prasanth Balakrishnan Nair
Air Commodore, Indian Air Force,
Astronaut-designate – Gaganyaan Human Spaceflight Mission, (ISRO), India

Shri Rahul Sharanappa Sankanur (IAS)
Director, Department of Electronics, Information Technology, Biotechnology, Science & Technology, Government of karnataka, EX Officio Managing Director, KITS

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Regional director for India, CUS, North America

Jayesh Tanwani
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Puneet Kumar Mishra
Director - Indian Space Research Organization Chair IEEE - AESS

Dr. Prasant Misra
Senior Scientist, TCS Research, Chair, IEEE Bangalore Section

Venkatakrishnan Janakiraman
CEO, QuarkCube

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Dr. V. V. Srinivasan
EX - ISTRAC, ISRO Professor of Practice,
Center for Space Science and Technology (CSST)

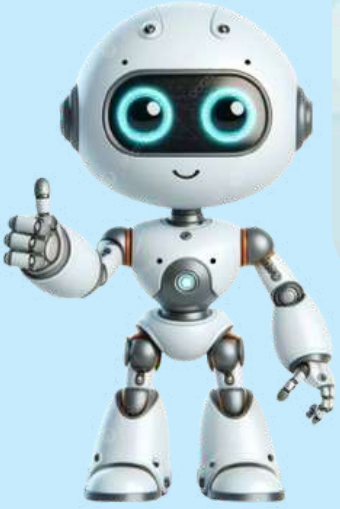
Avinash Vulasa
Senior Application Engineer, CoreEL Technologies, Mathworks products

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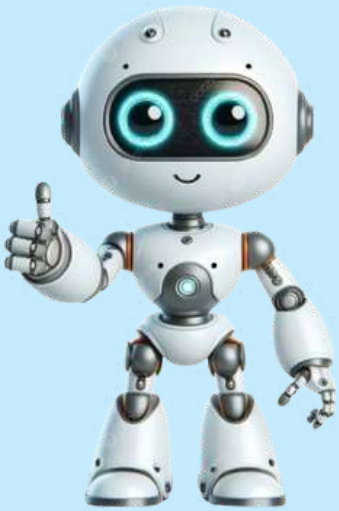
AWARDS AND RECOGNITIION

- Prize pool of ₹10 lakh for all major events.
- Free courses from Maven Silicon & EVE
- Placements worth ₹18 lakhs for all
- participants.
- All participants will receive: Certificates.




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23rd - 25th APRIL, 2026
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IEEE Signal Processing Society
CEDA
IEEE Information Theory Society
PAVAN HYUNDAI Just Happiness...!
Eve Placement
EVEPAPER
Dun Jun



DSU TECHFEST-CELESTAI

CelestAI'26, an International-Level Omni-Tech organized by Dayananda Sagar University, brought together young innovators from across India for an intensive 60 hours of creativity, collaboration, and hands-on learning. Aligned with the Sustainable Development Goals, the event provided a dynamic platform for students to ideate, design, and develop technology-driven solutions addressing real-world challenges. With expert mentorship from academia and industry, international academic collaboration, and enthusiastic student participation, CelestAI'26 successfully fostered innovation, interdisciplinary teamwork, and practical problem-solving in a highly engaging and professional environment.

OBJECTIVES

- To provide students with a national-level platform to showcase and develop their technical knowledge, innovation, creativity, problem-solving abilities, and practical skills through various technology-based events and competitions.
- Promote innovation and creativity among students.
- Develop practical and technical skills through hands-on competitions.
- Encourage problem-solving and teamwork.
- Bridge the gap between theoretical knowledge and real-world applications.
- Provide a PAN-India platform for students to interact, compete, and learn from peers.
- Inspire students to explore emerging technologies and build solutions for real-world challenges.


Department of Electronics and Communication Engineering
IEEE Circuits & Systems Society
IN COLLABORATION WITH
Department of Aerospace Engineering
Department of Computer Science Engineering (Data Science)
PRESENTS
DSU
CELESTAI
WHERE INNOVATION MEETS IMAGINATION
ROBOSOCCER
SKYRIFT
TECHZIBITION
ARTISTIC AURA
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WORKSHOP
23RD -25TH APRIL 2026
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Dr. Udaya Kumar Reddy K R, Dean-SOE, DSU
Convenors:
Dr. Arun Belodi, Professor & Chairperson-ECE, DSU
Dr.Nagaraja .S.R, Professor & Chairperson-AES, DSU

DSU TECHFEST-CELESTAI

HIGHLIGHTS

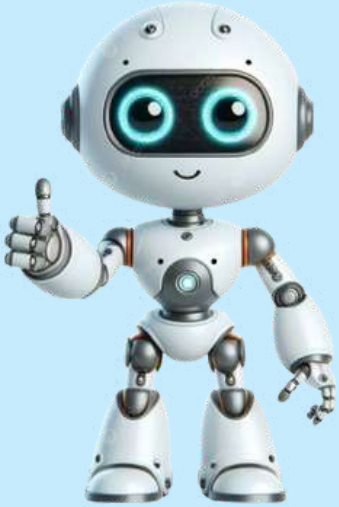
- National-Level Technical Platform: Brought together students from across India to participate in diverse technical and innovation-driven competitions.
- Promotion of Innovation & Creativity: Encouraged participants to transform ideas into practical, technology-driven solutions for real-world challenges.
- Hands-on Technical Exposure: Provided students with opportunities to apply AI, Data Science, Robotics, Electronics, Software Development, and Design concepts beyond the classroom.
- 24-Hour Intensive Hackathon: The Edge IQ Hackathon challenged participants to work continuously under strict time constraints, developing innovative solutions using AI, data analytics, and software technologies.
- Robotics & Engineering Excellence: Rover Rumble tested participants' expertise in robotic design, control systems, navigation, mechanical engineering, and real-time decision-making.
- Creative Design & User-Centric Thinking: The UI/UX Competition encouraged students to develop visually appealing, intuitive, and user-friendly solutions while applying design-thinking principles.
- Showcase of Student Innovation: Techzibition provided a prestigious platform for final-year students to exhibit their projects and demonstrate the practical application of their academic knowledge.
- Interdisciplinary Collaboration: Brought together students from ECE, Aerospace Engineering, Data Science, and other technical domains, encouraging cross-disciplinary learning and collaboration.
- Technical Knowledge Meets Adventure: Tech Quest transformed technical learning into an engaging treasure-hunt experience, testing logical reasoning, technical knowledge, teamwork, and quick thinking.
- Real-World Problem Solving: Events challenged students to address practical problems, strengthening their ability to analyze, design, develop, test, and present solutions.
- Teamwork & Leadership: Competitions fostered collaboration, leadership, communication, delegation, and effective coordination among participants.
- Innovation Under Pressure: Time-bound challenges enhanced students' ability to make quick, strategic, and effective decisions in high-pressure environments.
- Industry-Relevant Skills: Participants gained exposure to emerging technologies and practices that closely align with current industry requirements.
- Platform for Talent Recognition: Enabled students to showcase their technical expertise, creativity, and problem-solving abilities before judges, faculty, peers, and fellow participants.
- Knowledge Sharing & Networking: Created opportunities for students from different institutions and disciplines to interact, exchange ideas, and learn from one another.
- Confidence & Professional Development: Strengthened participants' confidence in presenting ideas, defending technical solutions, and working in competitive environments.
- From Ideas to Implementation: Emphasized the complete journey from concept generation to prototype development, problem-solving, and final presentation.
- Celebration of Emerging Technology: Established CELESTAI 2026 as a vibrant platform celebrating technology, innovation, creativity, engineering excellence, and the spirit of competition.




CELESTAI








CELESTAI
DSU TECHFEST



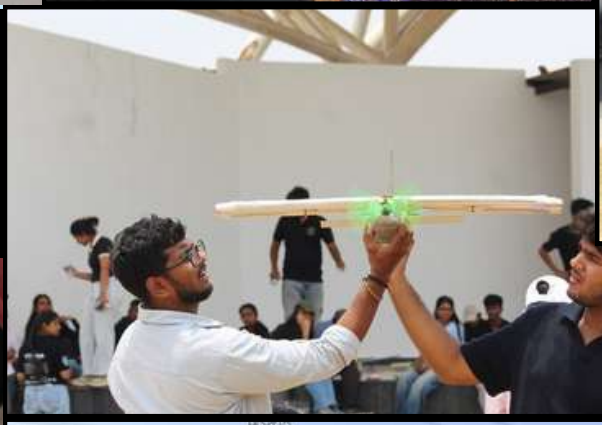


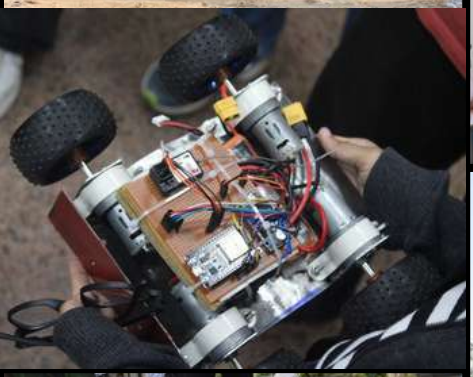












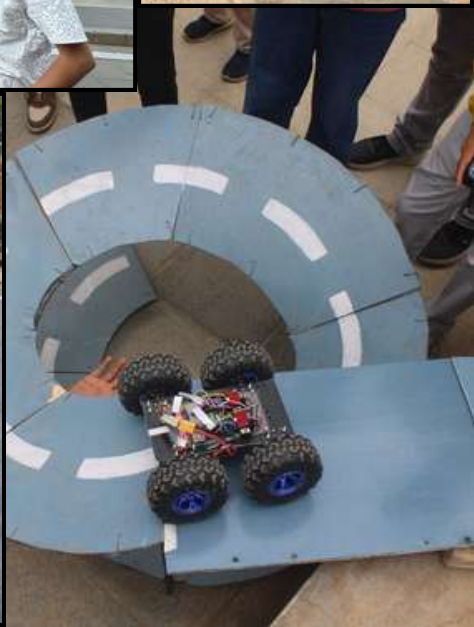





CELESTAI










PROMPT
WARS



















CONCLUSION

CELESTAI 2026 successfully provided a platform for innovation, technical excellence, creativity, and teamwork. The diverse events helped students apply their knowledge to real-world challenges, develop practical skills, and showcase their technical potential at a national level.



WINNERS - ROXX POWERBOTS, DSU



FIRST RUNNER UP - LATENCY ZERO, DSCE



SECOND RUNNER UP - PHANTOM STRIKERS, DSU

DSU TECHFEST-CELESTAI



WINNERS - V4, DSU



FIRST RUNNER UP - NEURAL NOMADS, DSU



SECOND RUNNER UP - TECH NEXUS NOVA, Vidyavardhaka College of Engineering

DSU TECHFEST-CELESTAI



WINNER - DARSHAN, DSU



WINNER - JATAYU, NITTE MEENAKSHI INSTITUTE OF TECHNOLOGY



WINNER - LUNAR_CODEX, DSU



WINNER - SVIT, SIR M VISVESWARAYA INSTITUTE OF TECHNOLOGY

DSU TECHFEST-CELESTAI



WINNER - UDAAN 47, MS RAMAIAH UNIVERSITY OF APPLIED SCIENCE

WINNER - KAJU KATLI, DSU





WINNER - NEXUS, DSU

WINNER - AYUDHAM, DSU



DSU TECHFEST-CELESTA!



WINNER - DUKES, DSU



WINNERS - ECEP110, ECE



WINNERS - PRJ25-003, ASE



WINNER - FRESH MINDER, CSE(DS)

FACULTY CO-ORDINATOR :
DR. DIVYASHREE H B, FACULTY ADVISOR,IEEE CASS, ECE, DSU

INVESTITURE CEREMONY

The IEEE Circuits and Systems Society (CASS) Student Branch Chapter Inauguration was held on 11 April 2026 at Dayananda Sagar University. The event marked the beginning of the CASS chapter at DSU, focusing on innovation, technical learning, research, and professional growth. It included an invocation song and lamp-lighting ceremony, expert insights on CASS, VLSI, and career opportunities, followed by the induction of the core committee. The event concluded with encouragement for students to actively participate, innovate, collaborate, and contribute to the growth of the chapter.

OBJECTIVES:

- Important Objectives of the Event
- To inaugurate the IEEE CASS Student Branch Chapter at Dayananda Sagar University.
- To promote innovation and research in circuits, systems, VLSI, and emerging technologies.
- To provide students with technical exposure through expert insights, workshops, hackathons, and industry interactions.
- To bridge the gap between academic knowledge and real-world applications.
- To develop professional skills such as leadership, teamwork, communication, and technical competence.
- To create networking opportunities with researchers, industry professionals, and IEEE members.
- To encourage students to actively participate in IEEE activities and contribute to the growth of the CASS chapter.



INVESTITURE CEREMONY





INVESTITURE CEREMONY







INVESTITURE CEREMONY

CONCLUSION:

The IEEE CASS Student Branch Chapter Inauguration at Dayananda Sagar University successfully marked the beginning of a platform for innovation, technical learning, research, and professional growth. The event inspired students to explore emerging technologies, develop practical skills, and actively participate in IEEE activities. It laid a strong foundation for future initiatives and the continued growth of the IEEE CASS chapter.



FACULTY CO-ORDINATOR : DR. DIVYASHREE H B, FACULTY ADVISOR,IEEE CASS, ECE, DSU

SKILL-SYNC

"Skill Sync: Engineering Futures – Unlock Your Global Career Potential" was an interactive session organized by IEEE and CASS at Dayananda Sagar University on 17 April 2026. The session guided students on global career opportunities, higher education, industry expectations, and essential technical and professional skills. The expert, Mr. Paul McBean, also highlighted the importance of practical experience, communication, adaptability, and continuous skill development.



CONCLUSION:

The session successfully guided students toward global career opportunities, skill development, and professional growth. It encouraged continuous learning, adaptability, and exploring international prospects for a successful career.



FACULTY CO-ORDINATOR :
Dr. DIVYASHREE H B, ASSISTANT PROFESSOR, ECE, DSU

Department Activities

CAREER PLANNING AND INDUSTRY READINESS

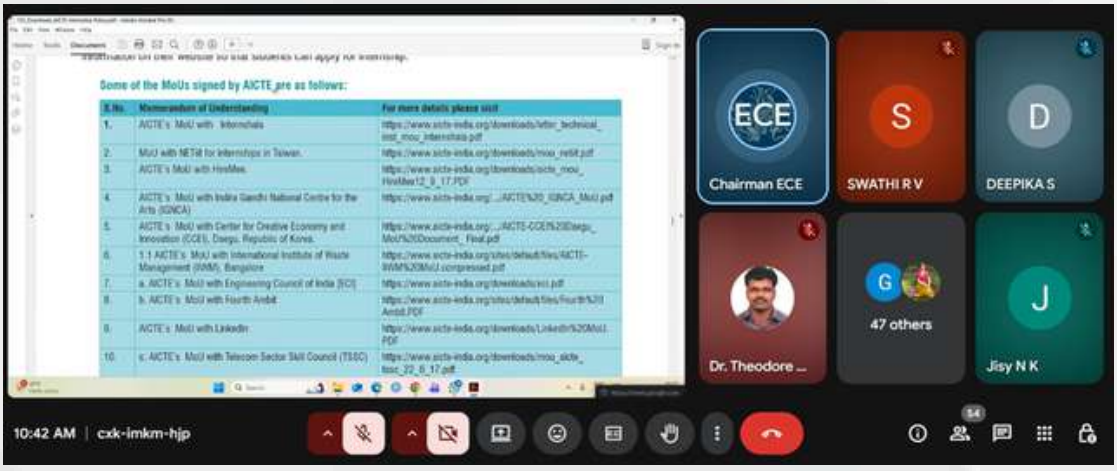
Dayananda Sagar University, Bengaluru was recognized by the IEEE Bangalore Section during the IEEE Bangalore Section AGM 2026 (Golden Jubilee Year) held on 18 January 2026. The University was ranked among the Top 25 IEEE Student Branches for outstanding contributions to IEEE membership growth and sustained activities, and also emerged as the Winner of the IEEE Bangalore Section Membership Development Committee (MDC) Challenge (1 October–18 November 2025). The recognition reflects the dedicated efforts of IEEE student and professional volunteers of the University.





The Department of Electronics and Communication Engineering (ECE), Dayananda Sagar University, organized a webinar titled “Career Planning and Industry Readiness” on 24 January 2026 for final-year B.Tech students (2022–2026 Batch). The session aimed to guide students in career planning, industry expectations, employability skills, and opportunities in higher studies, entrepreneurship, internships, and placements.

The session was delivered by Dr. Arun Balodi, Professor and Chairman, Department of ECE, who emphasized strategic career planning, continuous learning, adaptability, leadership, and aligning technical skills with industry requirements. Prof. Jisy N K welcomed the participants and introduced the speaker, while Dr. Theodore Chandra S actively supported the proceedings. The interactive webinar provided practical career guidance, enhanced employability awareness, and encouraged students to become industry-ready professionals.



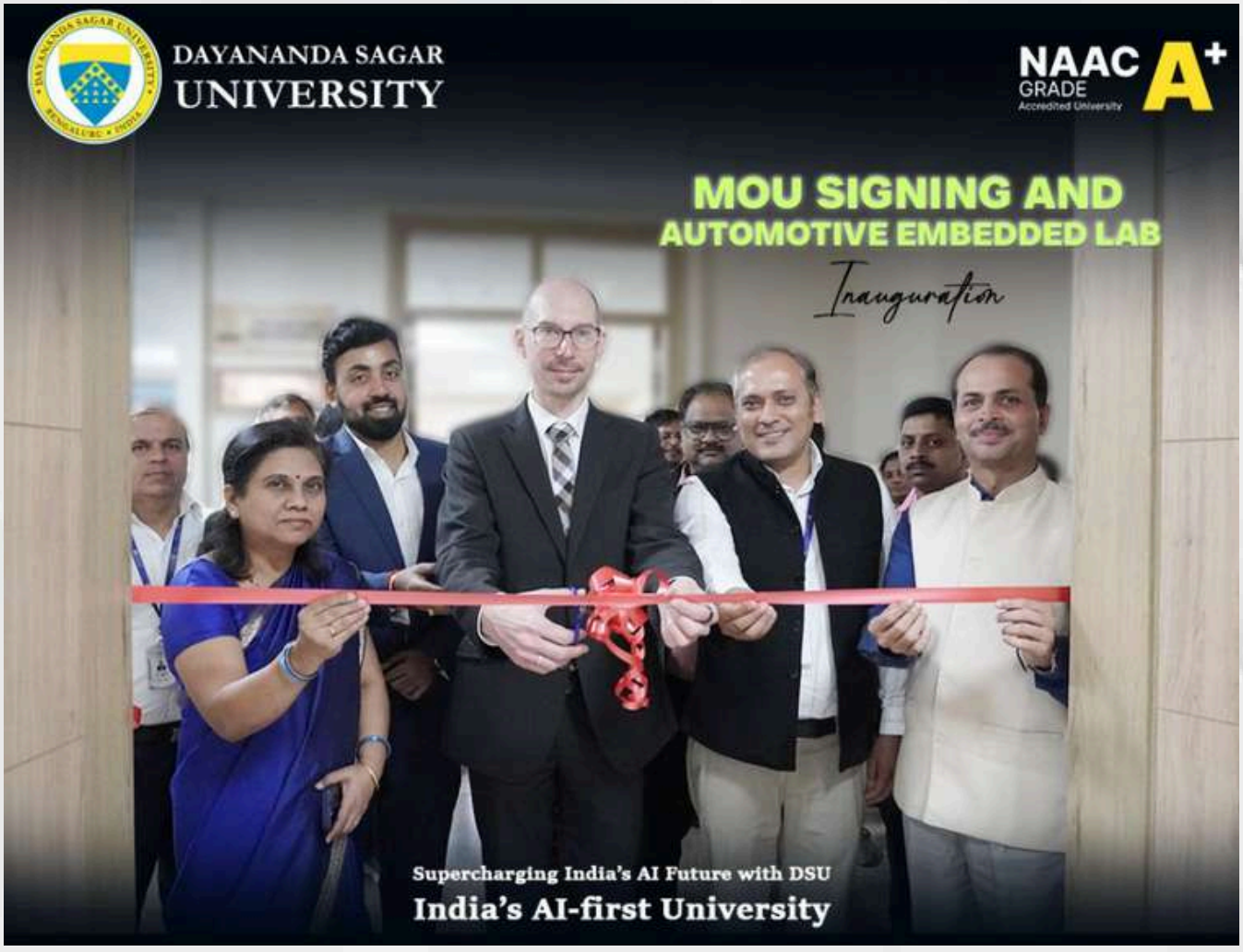


FACULTY CO-ORDINATOR :
DR. THEODORE CHANDRA S
MS. JISY N K

CONVENOR :
DR. ARUN BALODI,
CHAIRMAN OF ECE, DSU

VECTOR LAB INAGURATION

The Department of Electronics and Communication Engineering, Dayananda Sagar University, inaugurated the Automotive Embedded Systems Lab through an MoU with Vector Informatik India, supported by Tata Technologies' Automotive Engineering Capability Development initiative. The lab aims to bridge academia and industry through hands-on learning using advanced automotive embedded tools and technologies, fostering industry-ready engineers. The inauguration was graced by Shubhada Kanekal, Daniel Truer, and Keerthi Kumar, whose participation strengthened the academia–industry collaboration. This initiative reinforces the University's commitment to advanced engineering education and practical skill development.



FACULTY CO-ORDINATOR :
Mr. ABHINAV KARAN, ASSISTANT PROFESSOR, ECE, DSU

CAREER COUNSELLING

The Electroblitz Club of the Department of ECE, Dayananda Sagar University, organized “NextGen Futures: Strategic Career Guidance” on 24 February 2026 under the guidance of Dr. Divyashree H B. Conducted by Global Careers and delivered by Mr. Santosh, Branch Manager, the session focused on career planning, emerging technologies, higher studies, competitive examinations, certifications, internships, and skill development.

The talk provided practical insights into aligning academic learning with industry expectations, encouraging students to pursue continuous learning and goal-oriented professional growth.



FACULTY CO-ORDINATOR : DR. DIVYASHREE H B,
FACULTY ADVISOR,IEEE CASS, ECE, DSU

SKETCH THE INTELLIGENCE – AI IN EVERYDAY LIFE

The Department of Electronics and Communication Engineering, School of Engineering, Dayananda Sagar University, under the banner of Unity Hub, organized a Pencil Sketching Competition themed “AI in Everyday Life.” The event was coordinated by Dr. Navya R and Prof. Manasa K R.

The competition encouraged students to creatively depict the influence of Artificial Intelligence in everyday life through pencil art. Participants presented innovative sketches illustrating smart technologies, robotics, healthcare AI, and digital transformation. The event promoted creativity, attention to detail, and sustainable, low-resource artistic expression.

Dr. M. Shahina Parveen, Head of the Department, CST, Dayananda Sagar University, served as the judge and evaluated entries based on creativity, relevance to theme, technique, and presentation. The two-hour competition witnessed enthusiastic participation and successfully blended art with technological awareness, fostering innovation and holistic development among students.





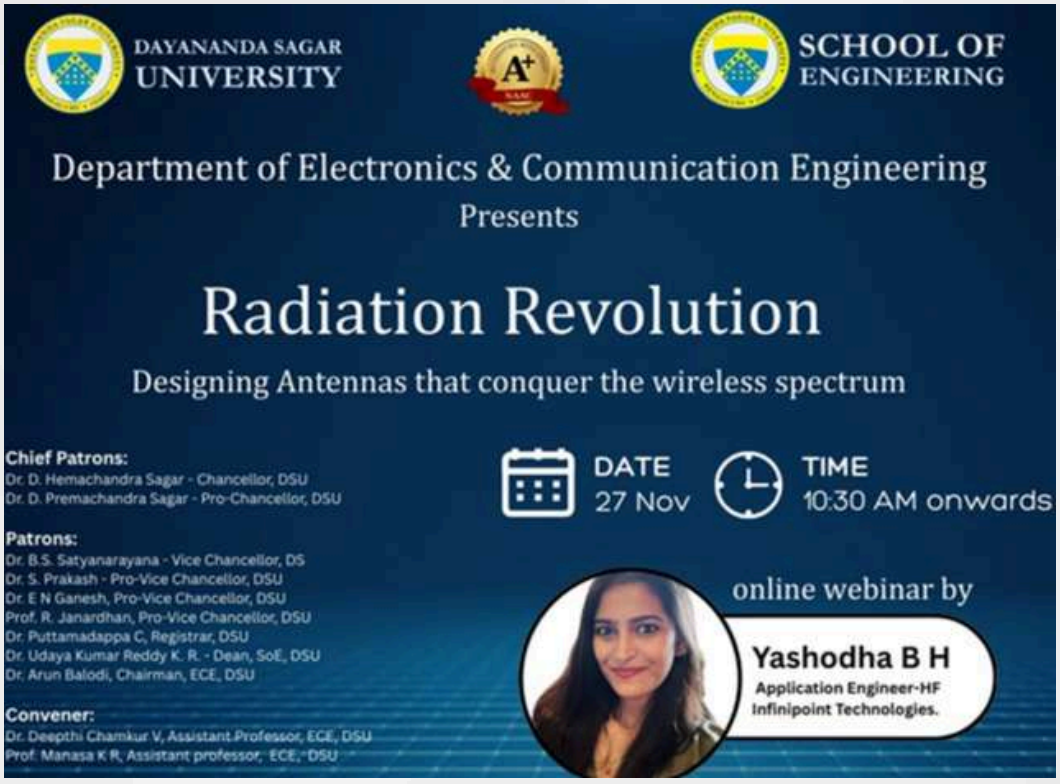


FACULTY CO-ORDINATOR :
DR. NAVYA R
PROF. MANASA K R
ASSISTANT PROFESSORS, ECE, DSU

RADIATION REVOLUTION: DESIGNING ANTENNAS THAT CONQUER THE WIRELESS SPECTRUM”

The Department of Electronics & Communication Engineering, School of Engineering, Dayananda Sagar University, organized an online webinar titled **“Radiation Revolution: Designing Antennas that Conquer the Wireless Spectrum.”** The session was delivered by **Yashodha B H**, Application Engineer – HF at Infini point Technologies.

The webinar focused on the vital role of antennas in modern communication, covering topics such as 5G, Massive MIMO, and millimetre-wave bands. Key design challenges including size constraints, beam steering, and system complexity were discussed, along with practical antenna solutions for 4G/5G devices. The session provided students with valuable industry insights and guidance on research, innovation, and high-frequency engineering applications, concluding with an engaging Q&A interaction.



FACULTY CO-ORDINATOR :
PROF. MANASA K R,
ASSISTANT PROFESSOR, ECE, DSU

EXPERT SESSION ON “VLSI DESIGN AND TEST”

The Department of ECE, Dayananda Sagar University, organized an expert session on “VLSI Design and Test” on 27 February 2026 at the VLSI Lab, in association with IEEE CASS and IEEE CEDA. Dr. Ravikumar CP, Chief Learning Officer, VinyanaTech, delivered insights into VLSI design flow, verification, validation, semiconductor industry roles, and essential engineering skills. Convened by Dr. Arun Balodi, the interactive session provided practical industry exposure and career guidance, reinforcing the department’s commitment to industry-oriented learning and semiconductor skill development.





FACULTY CO-ORDINATOR
AND
CONVENOR :
DR. ARUN BALODI,
CHAIRMAN OF ECE, DSU

SRI RAMA NAVAMI CELEBRATIONS

The Department of ECE celebrated Sri Rama Navami with devotion and cultural enthusiasm through a beautifully decorated display board featuring Lord Rama and traditional festive elements. Students actively participated in the decorations, showcasing creativity, teamwork, and cultural awareness. The celebration fostered unity, spiritual engagement, and appreciation of Indian cultural heritage beyond academics.

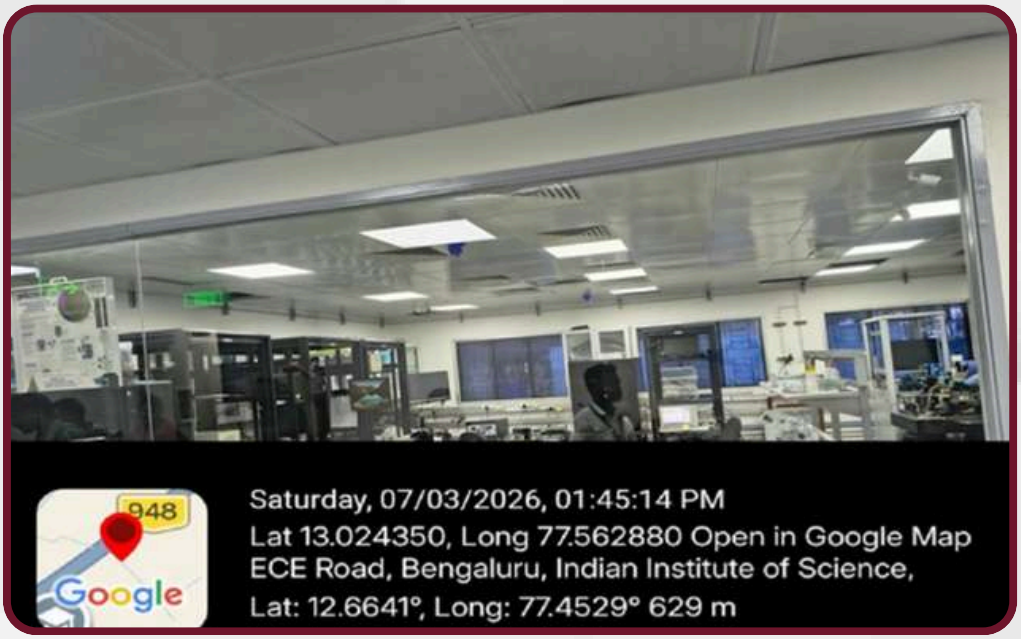




EDUCATIONAL VISIT TO IISC BANGALORE FAB LAB & MAVEN SILICON

The Department of ECE, Dayananda Sagar University, organized an educational visit to the IISc Fab Lab on 7 March 2025, in association with Maven Silicon, under the guidance of Dr. Divyashree H B and Mrs. Prabavathi. Students gained practical exposure to semiconductor fabrication, cleanroom facilities, and equipment such as photolithography, CVD, and SEM. Expert tutorials and exhibits on MEMS, biosensors, and nanotechnology enhanced their understanding of microelectronics and VLSI technologies.





FACULTY CO-ORDINATOR :
DR. DIVYASHREE H B,
FACULTY ADVISOR,IEEE CASS
MRS. PRABAVATHI
ASSISTANT PROFESSOR, ECE, DSU

EDUCATIONAL VISIT TO BHARAT ELECTRONICS LIMITED – CRL, BENGALURU

The Department of ECE, Dayananda Sagar University, organized an educational visit to BEL–CRL, Bengaluru, on 28 April 2026, led by Dr. Navya R and Dr. Pushpa Mala S, with 40 ECE and CSE students. Students gained exposure to advanced defence technologies, including radar systems, 5G/6G communication, AI/ML, robotics, and quantum technologies through technical sessions, live demonstrations, and interactions with experts. The visit strengthened practical understanding, highlighted indigenous technological advancements, and inspired students toward careers in engineering and research.

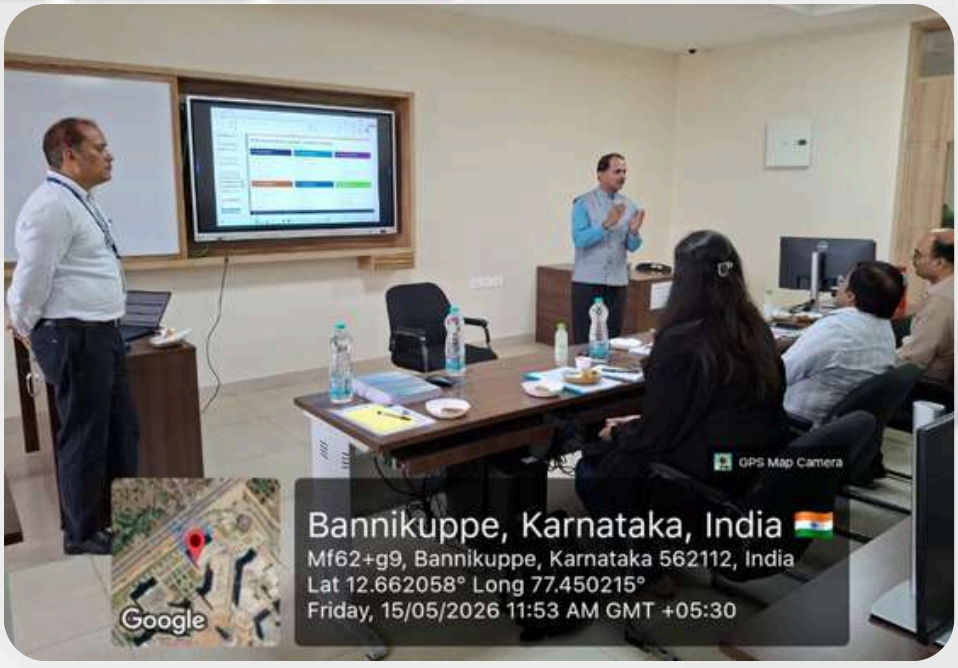


THE FACULTY COORDINATORS:
DR. NAVYA R, ASSISTANT PROFESSOR, ECE, DSU
DR. PUSHPA MALA S, ASSOCIATE PROFESSOR, ECE, DSU

13TH BOARD OF STUDIES (BOS) MEETING-ECE

The 13th Board of Studies (BoS) Meeting of the Department of ECE, Dayananda Sagar University, was held on 15 May 2026 under the chairmanship of Dr. Arun Balodi. Distinguished members from IISc Bengaluru, NIT Goa, MathWorks India, and BMW India participated in reviewing and approving the revised B.Tech ECE and M.Tech Embedded Systems curricula, emphasizing AI integration, industry collaboration, research excellence, and NEP 2020 compliance. The members appreciated the department's strategic initiatives, NVIDIA collaboration, industry partnerships, and outcome-based curriculum aimed at enhancing employability, innovation, entrepreneurship, and higher education opportunities.





FACULTY CO-ORDINATOR :
DR. ARUN BALODI,
CHAIRMAN OF ECE, DSU

FAREWELL CEREMONY FOR GRADUATING B.TECH AND M.TECH STUDENTS

The Department of ECE, Dayananda Sagar University, organized a farewell ceremony on 9 May 2026 for the outgoing B.Tech (2022–2026) and M.Tech (2024–2026) batches. The event celebrated students' academic achievements, friendships, and memorable experiences. Faculty members appreciated their dedication, innovation, and perseverance while extending best wishes for their future pursuits in higher studies, research, industry, and entrepreneurship. The ceremony concluded on a heartfelt note, encouraging graduates to continue learning, innovating, and contributing positively to society.





INDUSTRY INTERACTION WITH C-DOT ON INDIGENOUS TELECOM TECHNOLOGY AND COLLABORATION

The Department of ECE, DSU, participated in an industry interaction with C-DOT to explore collaboration in indigenous telecom solutions, including 4G/5G, cybersecurity, quantum communication, and AI-based network management. Discussions focused on joint proof-of-concept projects, technology transfer, and co-development aligned with BharatNet and Atmanirbhar Bharat. Faculty members **Dr. S. Arungalai Vendan, Dr. Pushpa Mala S, Dr. Sneha Sharma,** and **Dr. Deepthi Chamkur V** represented the department, strengthening academia–industry collaboration.



FACULTY CO-ORDINATOR :
Dr. PUSPHA MALA S,
ASSOCIATE PROFESSOR, ECE,
DSU

CELESTAI'26 RECEIVES GLOBAL RECOGNITION

The Department of Electronics and Communication Engineering, Dayananda Sagar University, takes pride in the global recognition received for its flagship TechFest, CELESTAI'26, by Edge Impulse. The recognition highlights the event's contribution to promoting Edge AI, Embedded Systems, Robotics, and emerging technologies among students. A special appreciation goes to student Vikram Adhitya, whose efforts as an Edge Impulse Campus Ambassador helped strengthen industry engagement and provide students with exposure to cutting-edge technologies.



Faculty Achievements

Dr. Arun Balodi

Dr. Arun Balodi represented IEEE SPS, Bangalore Chapter, as Session Chair at IITCEE 2026, held on 22 January 2026 at BNM Institute of Technology, Bengaluru, contributing to research presentations and technical discussions.





Dr. Arun Balodi served as Session Chair at IEEE ICAUC 2026, held on 21 January 2026 at Shinawatra University, Thailand, contributing to research discussions on AI-driven smart systems and ubiquitous computing while fostering academic collaboration.

Dr. Arun Balodi attended the IEEE Bangalore Section AGM 2026 on 18 January as an Executive Committee Member. The meeting highlighted the Section's achievements, membership growth, technical initiatives, transparent governance, and recognition of award-winning chapters, including IEEE SPS and IEEE VTS Bangalore.



Dr. Arun Balodi was inducted as an Executive Committee Member of the IEEE CEDA Bangalore Chapter for 2026, contributing to technical initiatives, workshops, and professional engagement in Electronic Design Automation (EDA).





Dr. Arun Balodi received a Certificate of Appreciation as an IEEE Day 2025 Ambassador for promoting technical excellence and community engagement across IEEE Region 10 and the Bangalore Section.

Dr. Arun Balodi received a Certificate of Appreciation for serving as Session Chair at EPREC-2026, held at IIT Bhilai from 2–4 January 2026, contributing to technical discussions and session coordination.



Dr. Arun Balodi, Department of ECE, DSU, was appointed Technical Program Committee (TPC) Chair for BDMLIC 2026, Shenzhen, China, overseeing technical reviews and contributing to the conference program.


ICOMD

CERTIFICATE

OF APPOINTMENT

THIS CERTIFICATE IS PROUDLY AWARDED TO

Prof. Arun Balodi

From Dayananda Sagar University, India

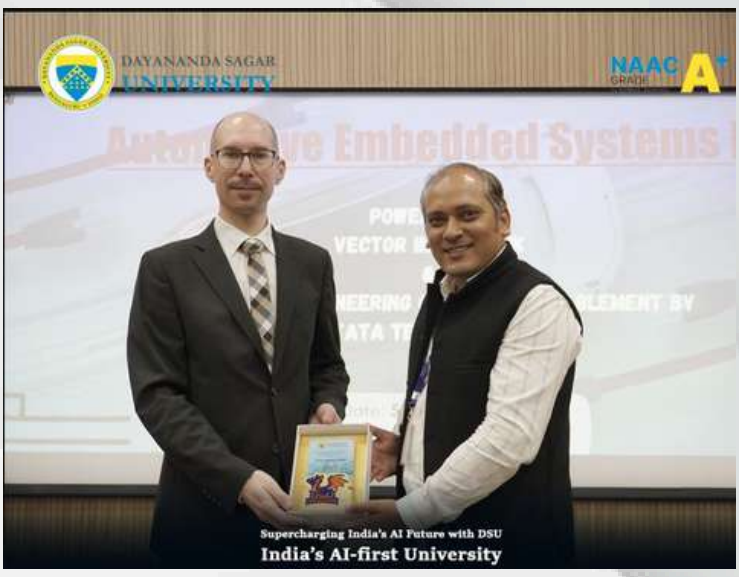
Who has been invited as the

Technical Program Committee Chair

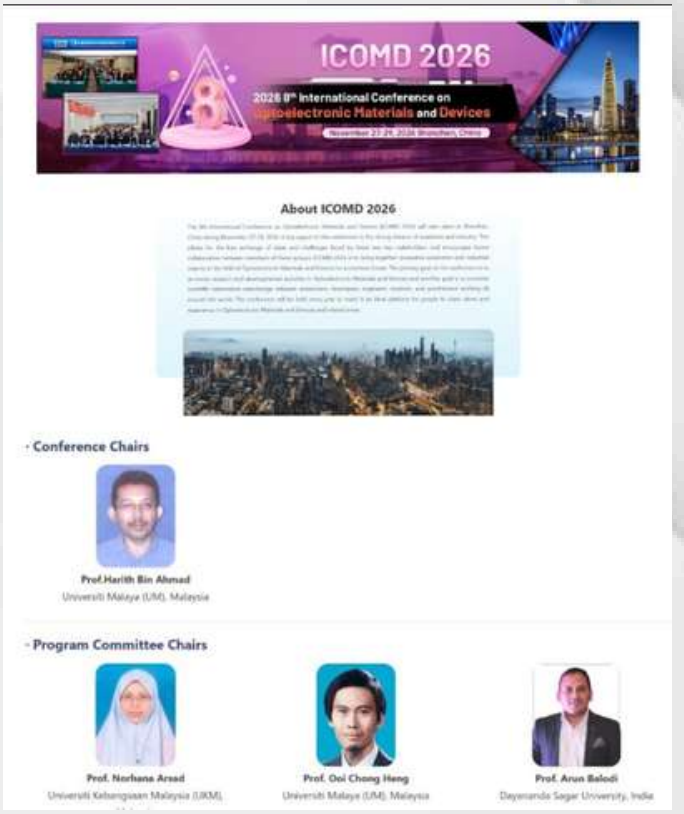
of 2026 8th International Conference on Optoelectronic Materials and Devices (ICOMD 2026)

November 27 to 29, 2026 | Shenzhen, China

Dr. Arun Balodi, Professor and Chairperson, ECE, DSU, was recognized for his role as Conference Chair at an international conference, acknowledging his leadership and contributions to research and academic collaboration.



Dr. Arun Balodi, Professor and Chairperson, ECE, DSU, was appointed Technical Program Committee Chair for ICOMD 2026, scheduled for 27–29 November 2026 in Shenzhen, China, recognizing his expertise and contributions.



Dr. Arun Balodi received a Certificate of Appreciation for serving as Program Track Chair at the IEEE IMED Conference 2026, held on 6–7 March at Jesselton University College, Malaysia, recognizing his academic contributions and international research engagement.





Dr. Arun Balodi, Professor and Chairperson, ECE, DSU, participated in the IEEE Bangalore Section Golden Jubilee Celebration at Taj Vivanta, Bengaluru, commemorating 50 years of innovation, professional growth, and technological collaboration.

Dr. Arun Balodi, Professor and Chairperson, ECE, DSU, was recognized as an Executive Board Member of the STEM Research Society for his contributions to research and academic leadership.



Dr. Arun Balodi, Professor and Chairperson, ECE, DSU, attended IEEE BHTC 2026, exploring technology-driven solutions in healthcare, sustainability, and rural development while promoting AI-driven healthcare, collaborative research, and humanitarian innovation.



Dr. Arun Balodi, Professor and Chairman, ECE, DSU, delivered two expert sessions on 10 May 2026 at ISME, Bengaluru, under the Diploma in Professor of Practice programme. The sessions focused on interactive course materials, technology-enabled teaching, and hybrid learning practices, promoting pedagogical innovation and faculty development.



Dr. Arun Balodi, Professor and Chairperson, ECE, DSU, participated in the IEEE CEDA SMS 2026 on 28 June in Bengaluru, gaining insights into semiconductor manufacturing, AI-enabled design, and industry–academia collaboration.



Dr. Arun Balodi, Professor and Chairperson, ECE, DSU, delivered a keynote address at the IEEE International Workshop on Metrology for Automotive 2026 in Brescia, Italy, highlighting the department's global academic engagement and commitment to research and innovation.



Dr. Pushpa Mala

Dr. Pushpa Mala S received the IEEE WIE Bangalore Section Outstanding WIE Professional (Academia) Award – 2025 for her leadership, dedicated service, and contributions to empowering women in engineering.



Dr. Pushpa Mala S, Department of ECE, served as a resource person for the NBA Awareness Faculty Development Program on 29 January 2026, delivering a session on CO–PO Mapping to enhance outcome-based technical education.



Dr. Pushpa Mala S, Department of ECE, delivered a talk titled “Use of AI Tools and Digital Pedagogy” at the IEEE Outreach Summit on 21 February 2026 at IISc, Bengaluru, highlighting AI-driven education and digital innovation for enhanced learning and humanitarian outreach.



‘ಎಲ್ಲರಿಗೂ ಬೇಕು ಉದಯೋನ್ಮುಖ ತಂತ್ರಜ್ಞಾನ’

ಪ್ರಜಾವಾಣಿ ವಾರ್ತೆ

ನಾಯಕನಹಟ್ಟಿ: 'ಗ್ರಾಮೀಣ ಭಾಗದ ಎಲ್ಲಾ ವಿದ್ಯಾರ್ಥಿಗಳು ಮತ್ತು ಅಧ್ಯಾಪಕರಿಗೆ ಉದಯೋನ್ಮುಖ ತಂತ್ರಜ್ಞಾನ ಮತ್ತು ವೃತ್ತಿಪರ ಕೌಶಲದ ಜ್ಞಾನ ದೊರಕಿಸಿಕೊಡುವ ನಿಟ್ಟಿನಲ್ಲಿ ತರುವೇತಿ ಕಾರ್ಯಾಗಾರವನ್ನು ಹಮ್ಮಿಕೊಳ್ಳಲಾಗಿದೆ' ಎಂದು ಐಐಎಸ್ ಮುಖ್ಯಸ್ಥರಿ. ಸುಬ್ಬಾರೆಡ್ಡಿ ಹೇಳಿದರು.

ಹೋಬಳಿಯ ಕುದಾಪುರದ ಐಐಎಸ್ ಕ್ಯಾಂಪಸ್‌ನಲ್ಲಿ ಶನಿವಾರ ಆಂತರರಾಷ್ಟ್ರೀಯ ಮಟ್ಟದ ಐಇಇ ವಿಜ್ಞಾನ ಸಂಸ್ಥೆಯ ಮಾನವಿಕ ವಿಜ್ಞಾನ ವಿಭಾಗದಿಂದ ನಡೆದ ಉದಯೋನ್ಮುಖ ತಂತ್ರಜ್ಞಾನ ಮತ್ತು ವೃತ್ತಿಪರ ಕೌಶಲ ಅಭಿವೃದ್ಧಿಯ ಬಗ್ಗೆ ಒಂದು ದಿನದ ತರಬೇತಿ ಕಾರ್ಯಾಗಾರದಲ್ಲಿ ಮಾತನಾಡಿದರು.

'ಇತ್ತೀಚಿನ ದಿನಗಳಲ್ಲಿ ವಿಜ್ಞಾನ ಕ್ಷೇತ್ರದಲ್ಲಿ ಕೃತಕ ಬುದ್ಧಿಮತ್ತೆ (ಎಐ), ಕ್ವಾಂಟಮ್ ಕಂಪ್ಯೂಟಿಂಗ್, ನವೀಕರಿಸಬಹುದಾದ ಇಂಧನ, ಬಯೋ ಮೆಡಿಕಲ್ ಎಂಜಿನಿಯರಿಂಗ್ ಮುಂತಾದ ತಂತ್ರಜ್ಞಾನ ಕ್ಷೇತ್ರಗಳಲ್ಲಿ ಮಹತ್ತರವಾದ ಬೆಳವಣಿಗೆ ಕಂಡುಬರುತ್ತಿವೆ. ಅಂತರರಾಷ್ಟ್ರೀಯ ಮಟ್ಟದ ವಿಜ್ಞಾನ ಸಂಸ್ಥೆಗಳು ಇಂತಹ ಜ್ಞಾನ ಶಾಖೆಗಳ ಬಗ್ಗೆ ನಗರಗಳಲ್ಲಿ ತರುವೇತಿ, ಕಾರ್ಯಾಗಾರಗಳನ್ನು ನಡೆಸುತ್ತವೆ. ಆದರೆ, ಗ್ರಾಮೀಣ ಭಾಗದಲ್ಲಿ ಕಲಿಯುತ್ತಿರುವ ಎಂಜಿನಿಯರಿಂಗ್ ವಿದ್ಯಾರ್ಥಿಗಳಿಗೆ ಮತ್ತು ಅಧ್ಯಾಪಕರಿಗೆ ಉದಯೋನ್ಮುಖ ತಂತ್ರಜ್ಞಾನ ಮತ್ತು ಕೌಶಲಗಳು ದೊರಕುವುದಿಲ್ಲ. ಹಾಗಾಗಿ ಐಐಎಸ್ ಕ್ಯಾಂಪಸ್‌ನಲ್ಲಿ ಬೆಂಗಳೂರಿನಲ್ಲಿರುವ ಆಂತರರಾಷ್ಟ್ರೀಯ ಮಟ್ಟದ ಇಲೆಕ್ಟ್ರಿಕಲ್ ಅಂಡ್ ಇಲೆಕ್ಟ್ರಾನಿಕ್ಸ್ ಎಂಜಿನಿಯರಿಂಗ್ ಸಂಸ್ಥೆಯ ಸಹಯೋಗದಲ್ಲಿ ತರುವೇತಿ ಕಾರ್ಯಾಗಾರವನ್ನು ಹಮ್ಮಿಕೊಳ್ಳಲಾಗಿದೆ' ಎಂದು ತಿಳಿಸಿದರು.

'ಇದರಿಂದ ಚಳ್ಳಕೆರೆ, ಚಿತ್ರದುರ್ಗ, ರಾಯಚೂರು, ಬಳ್ಳಾರಿ, ವಿಜಯನಗರ, ತುಮಕೂರು ಭಾಗದಲ್ಲಿರುವ ಎಂಜಿನಿಯರಿಂಗ್ ಕಾಲೇಜುಗಳ ವಿದ್ಯಾರ್ಥಿಗಳು ಮತ್ತು ಅಧ್ಯಾಪಕರಿಗೆ ಶೈಕ್ಷಣಿಕ ಕ್ಷೇತ್ರದಲ್ಲಿ ಎಐ ಮತ್ತು ಕ್ವಾಂಟಮ್ ಕಂಪ್ಯೂಟಿಂಗ್ ವಿಷಯ ಬಗ್ಗೆ ತಿಳಿದುಕೊಳ್ಳಲು ಸಹಕಾರಿಯಾಗುತ್ತಿದೆ. ಬಳಿಕ ವತಿಯಿಂದ ಇನ್ನೂ ಹಲವು

ನಾಯಕನಹಟ್ಟಿ ಸಮೀಪದ ಕುದಾಪುರ ಐಐಎಸ್ ಪ್ರತಿಭಾನ್ವೇಷಣೆ ಮತ್ತು ಕೌಶಲಾಭಿವೃದ್ಧಿ ಕೇಂದ್ರದಲ್ಲಿ ಶನಿವಾರ ಉದಯೋನ್ಮುಖ ತಂತ್ರಜ್ಞಾನ ಮತ್ತು ವೃತ್ತಿಪರ ಕೌಶಲ ಅಭಿವೃದ್ಧಿ ತರುವೇತಿ ಕಾರ್ಯಾಗಾರ ನಡೆಯುತು

ಕಾರ್ಯಾಗಾರಗಳನ್ನು ಐಐಎಸ್ ಕ್ಯಾಂಪಸ್‌ನಲ್ಲಿ ಹಮ್ಮಿಕೊಳ್ಳಲಾಗುವುದು' ಎಂದರು.

ಇದೇ ವೇಳೆ ಕಾರ್ಯಾಗಾರದಲ್ಲಿ ಬೆಂಗಳೂರಿನ ಎಐಇ ಸಂಸ್ಥೆಯ ಆನಂದಿ ಗಿರಿಧರನ್ ಅವರು ಸಂಸ್ಥೆಯ ಕಾರ್ಯವ್ಯಾಪ್ತಿ ಮತ್ತು ಉದ್ದೇಶವನ್ನು ವಿವರಿಸಿದರು.

ಪ್ರೊ.ಲೀಲಾ ಚಂದ್ರಶೇಖರ್ ಕೃತಕ ಬುದ್ಧಿಮತ್ತೆ ಚಾಲಿತ ತರುವೇತಿ, ದಯಾನಂದ ಸಾಗರ್ ವಿಶ್ವವಿದ್ಯಾಲಯದ ಪ್ರೊ.ಪುಷ್ಪಮಾಲಾ ಅವರು ಎಐ ಪರಿಕರಗಳ ಬಳಕೆ ಮತ್ತು ಡಿಜಿಟಲ್ ಶಿಕ್ಷಣಶಾಸ್ತ್ರವನ್ನು ಕುರಿತು ತಾಂತ್ರಿಕ ಚರ್ಚೆ ನಡೆಸಿದರೆ, ರಾಜೇಶ್ವರಿ ಸುಬ್ಬೂರಿ ಅವರು ಎಐ ಜೊತೆ ಸಂಯೋಜಿಸಲ್ಪಟ್ಟ ಬಯೋಮೆಡಿಕಲ್ ಸಾಧನಗಳ ಅಭಿವೃದ್ಧಿ, ಪ್ರವೀಣ್ ಅವರು 5ಜಿ ಮತ್ತು ಆಟೆ ತಂತ್ರಜ್ಞಾನ, ಪ್ರೊ.ಸತ್ಯನಾರಾಯಣ ಅವರು ವೈರ್‌ಲೆಸ್ ಸೆನ್ಸರ್ ನೆಟ್‌ವರ್ಕ್‌ಗಳಿಗೆ ಭದ್ರತಾ ನೆಲಗುಟ್ಟು ವಿಷಯದ ಬಗ್ಗೆ ಚರ್ಚಿಸಿದರು.



Dr. Pushpa Mala S attended the IEEE Conference Organizers Education Workshop organized by IEEE Bangalore Section on 2 February 2026 at Hotel Hilton, strengthening her expertise in conference organization and global academic standards.





IEEE BANGALORE SECTION

Conference Organizers Education Workshop - 2026

CERTIFICATE

OF PARTICIPATION

This Certificate is presented to

Pushpa Mala S.

from Dayananda Sagar University

for participating in the Conference Organizers Education Workshop (COEW) - 2026 organized by IEEE Bangalore Section on 2nd February 2026

Dr. S. V. Sathyanarayana
Vice Chair (Technical Activities)
IEEE Bangalore Section

Dr. Prasant Misra
Chair
IEEE Bangalore Section

Dr Pushpa Mala S participated in the IEEE 50 yr celebration held at Taj Yeshwantpur on 26-04-2026. She serves as the IEEE EXECOM member Bangalore section.



Dr Pushpa Mala S is nominated as the publicity chair for the IEEE TEMS Asia pacific conference - TEMSCON 2026

Publicity Chairs

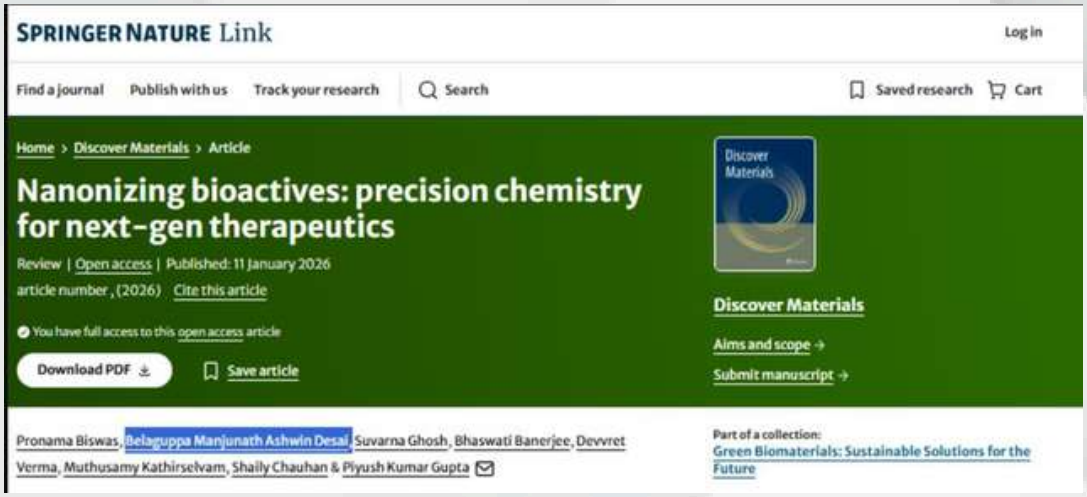
Jeffrey T. Dellosa Caraga State University, Philippines	Pushpa Mala S Dayananda Sagar University, Banglore, India	Kirtirajsinh Zala Marwadi University, Rajkot, India



Dr. Pushpa Mala S participated in the Golden Jubilee IEEE India Council Celebrations in Varanasi (23–24 May 2026) and served as a Jury Member for the Elevate NXT 2026 Pitching Round on 18th of May, supporting professional collaboration and entrepreneurial innovation.

Dr. Ashwin Desai B M

Dr. Ashwin Desai B M published the review article “Nanonizing Bioactives: Precision Chemistry for Next-Gen Therapeutics” in Discover Materials (Springer Nature) in January 2026, following three years of collaborative research.



Dayananda Sagar University received AICTE RPS – Lab to Market funding of ₹19 lakh for the project “Development of Portable Electrospinning Device & Biocompatible Formulations for In-situ Application of Nanofibers for Wound Management.” Led by Dr. BM Ashwin Desai (PI) and Dr. Pronama Biswas (Co-PI), the project aims to advance innovative healthcare solutions and achieve TRL 6/7, bridging laboratory research with market-ready applications.


AICTE RPS (Lab to Market) Project Sanction – Intimation & Congratulations External Inbox ×

Chairman ECE via googlegroups.com Mar 26, 2026, 8:08 PM (5 days ago)
to B, Prakash, Registrar, Udaya, Dean, Supriya, Director-IQAC, chairpersons-soe, dsuecefaculty, Ashwin, Pronama

Respected Sir,

Greetings of the day

I am pleased to inform you that a research proposal from our institution has been **approved under the All India Council for Technical Education (AICTE) RPS – Lab to Market Scheme**.

Project Title:
Development of Portable Electrospinning Device & Biocompatible Formulations for In-situ Application of Nanofibers for Wound Management

Application ID: RPS-1-7324150851-2025-6854
Sanctioned Budget: ₹19,00,000

Principal Investigator (PI):
Dr. BM Ashwin Desai (ECE – School of Engineering)

Co-Principal Investigator (Co-PI):
Dr. Pronama Biswas (Genetics – SBAS)

The project has been recognized for its strong translational potential and is expected to achieve **Technology Readiness Level (TRL) 6/7**, contributing significantly toward bridging the gap between laboratory research and market-ready solutions, particularly in the healthcare domain.

Dr. Vinu R

Dr. Vinu R, Associate Professor, ECE, DSU, co-authored the research paper “An Integrated Sensor-Based Machine Learning System for Predicting Crops and Fertilizers,” presented at IEEE INDICON 2025, Bengaluru, contributing to research in sensor-based machine learning for agriculture.



Conferences > 2025 IEEE 22nd India Council ...

An Integrated Sensor-Based Machine Learning System for Predicting Crops and Fertilizers

Publisher: IEEE | Cite This | PDF

Sumaiya MN ; Vinu R ; Sriatha Y ; Syed Ateequr Rehman ; Sindhu K ; Kavyashri G All Authors

11 Full Text Views

Abstract

Document Sections

I. Introduction

II. Materials and Methodology

III. Experimental Results and Discussion

IV. Conclusion

Authors

Figures

References

Keywords

Metrics

Abstract:

Selecting suitable crops based on soil nutrient composition, including nitrogen (N), phosphorus (P), potassium (K), and other essential elements, is a significant challenge for farmers. Traditional soil testing methods are time-consuming, requiring several weeks for laboratory results, and often do not include crop recommendations. To address this issue, we propose a system integrating sensor technology with machine learning algorithms such as Random Forest, Naive Bayes, and KNN classifiers to analyse soil properties in real time. Sensors measure key soil parameters such as N, P, K, pH, temperature, and humidity, transmitting real time data to three machine learning models implemented in Python. The proposed system then predicts three optimal fertilizer and crop choices, enhancing both yield and soil sustainability. Instead of suggesting generic fertilizers, the model detects nutrient deficiencies and recommends only the necessary supplements. Using multiple algorithms, it generates three crop and fertilizer options, giving farmers the flexibility to choose the best fit for their needs. For random data samples collected from nearby our areas, proposed method predicts Nitrogen, Phosphorous, Potassium and pH with the accuracy of 95.24%, 97.96%, 97.23% and 100% respectively.

Published in: 2025 IEEE 22nd India Council International Conference (INDICON)

Date of Conference: 18-20 December 2025

DOI: 10.1109/INDICON68490.2025.11392969

Date Added to IEEE *Xplore*: 20 February 2026

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Single-event transient analysis on radiation-hardened SiGe and GaN ringfet's using 3D TCAD simulations

Research | Open access | Published: 06 March 2026

article number , (2026) | Cite this article

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Discover Materials

R. Vinu

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Sections | References

Abstract

Data availability

Dr. Vinu.R, Associate Professor, Department of ECE, Dayananda Sagar University, has co-authored a research paper titled “Single-event transient analysis on radiation-hardened SiGe and GaN ringfet's using 3D TCAD simulations” published in Discover Materials. 2026 Mar 6, https://doi.org/10.1007/s43939-026-00592-9

Dr. Owais Ahmad Shah

Dr. Owais Ahmad Shah has published his research article, "A CNTFET Based Process Variation Resilient SRAM Design for Stable Low Power and Half Select Free Operation," in the prestigious Scientific Reports journal, published by Nature Portfolio. The research presents an innovative low-power SRAM design using CNTFET technology, offering improved stability, reliability, and energy efficiency for next-generation nanoscale memory systems. This achievement reflects Dr. Owais's contribution to high-impact research and excellence in semiconductor and VLSI technologies.



scientific reports

OPEN

A CNTFET based process variation resilient SRAM design for stable low power and half select free operation

Shams Ul Haq[1], Alireza Aminzadeh[2], Abdolreza Darabi[3], Erfan Abbasian[4], Owais Ahmad Shah[5] & Vakkalakula Bharath Sreenivasulu[6]

Static random-access memory (SRAM) design at nanoscale dimensions faces critical challenges arising from degraded stability, excessive power dissipation, and heightened sensitivity to process variations, particularly under low-voltage operation. To address these limitations, this paper proposes a robust and energy-efficient carbon nanotube field-effect transistor (CNTFET)-based nine-transistor (9T) SRAM cell architecture optimized for low-power applications. The proposed design employs a fully decoupled read and write structure with a single-ended access scheme, effectively eliminating read-disturb and half-select failures while enhancing overall noise immunity. Read stability is significantly improved by isolating the storage nodes from the read bitline, enabling the read static noise margin (RSNM) to reach the hold static noise margin (HSNM). Write robustness is achieved through controlled manipulation of the inverter pull-down paths, facilitating conflict-free write operations without aggressive transistor upsizing or complex assist circuitry. HSPICE simulations using the Stanford 32-nm CNTFET model demonstrate that, at a supply voltage of 0.3 V, the proposed SRAM achieves a 2.1 × improvement in RSNM and over a 14 × enhancement in write static noise margin (WSNM) compared to the conventional 6T SRAM. In addition, reduced bitline activity, elimination of precharge circuitry, and effective transistor stacking result in substantial reductions in read, write, and leakage power consumption. Monte Carlo simulations incorporating realistic process variations further confirm superior robustness, with the highest mean-to-standard-deviation ratios for both RSNM and WSNM among the compared designs. Layout-level evaluation shows that these benefits are achieved with only a modest area overhead relative to the 6T SRAM cell and with a smaller footprint than existing 9T and 10T alternatives. Overall, the proposed CNTFET-based 9T SRAM cell provides a well-balanced solution for low-voltage, energy-constrained, and variability-aware memory systems, making it a promising candidate for future CNTFET-based integrated circuits.

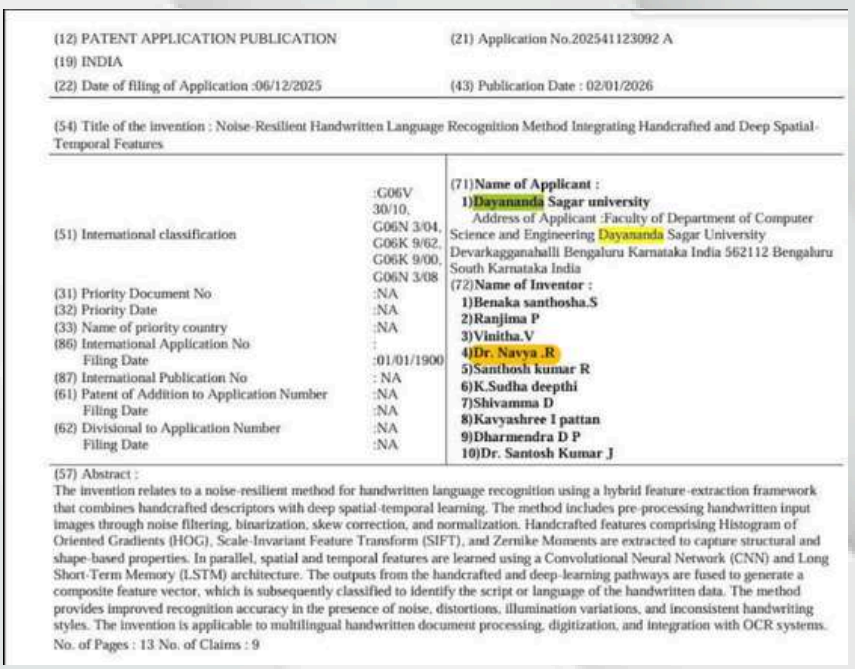
Keywords SRAM, Carbon nanotube FETs, Low power, Monte-Carlo simulation, Single-ended structure

The proliferation of internet of things (IoT) applications has led to an exponential increase in the deployment of wireless sensor nodes, which form the foundational layer of pervasive sensing networks. These nodes, often operating under stringent energy budgets harvested from their environment, necessitate ultra-low-power system-on-chip (SoC) designs[1]. Embedded static random-access memories are indispensable components in these sensor interfaces, data processors, and communication modules, occupying a substantial portion of the chip area and dominating the overall power consumption and performance[2]. Nowadays, the trend of continuous and intensive scaling of technology nodes towards single digits has provided significant challenges in designing SRAM architectures in SoC platforms with a significant share of area for very large-scale integration (VLSI) circuit designers[3]. These challenges include data-dependent leakage in the read path, write degradation,

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Dr. Navya R

Dr. Navya R, Assistant Professor, ECE, DSU, secured an Indian patent for “Noise-Resilient Handwritten Language Recognition Method Integrating Handcrafted and Deep Spatial-Temporal Features,” advancing research in hybrid deep learning and handwritten language recognition.



(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :06/12/2025

(21) Application No.202541123092 A
(43) Publication Date : 02/01/2026

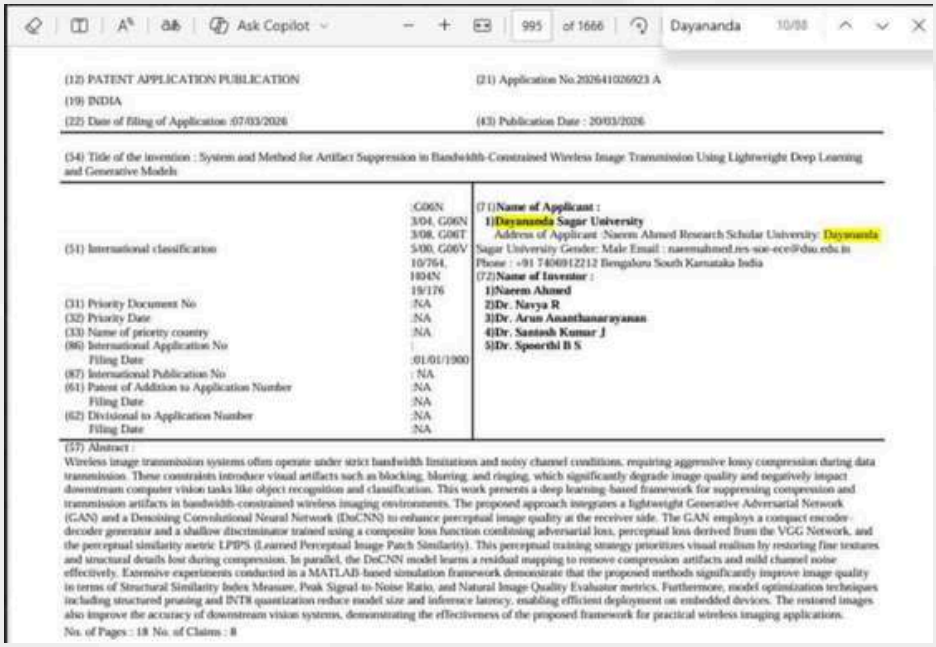
(54) Title of the invention : Noise-Resilient Handwritten Language Recognition Method Integrating Handcrafted and Deep Spatial-Temporal Features

(51) International classification :G06V 30/10, G06N 3/04, G06K 9/62, G06K 9/00, G06N 3/08
(31) Priority Document No :NA
(32) Priority Date :NA
(33) Name of priority country :NA
(86) International Application No : Filing Date :01/01/1900
(87) International Publication No : NA
(61) Patent of Addition to Application Number :NA Filing Date :NA
(62) Divisional to Application Number :NA Filing Date :NA

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10)Dr. Santosh Kumar J

(57) Abstract :
The invention relates to a noise-resilient method for handwritten language recognition using a hybrid feature-extraction framework that combines handcrafted descriptors with deep spatial-temporal learning. The method includes pre-processing handwritten input images through noise filtering, binarization, skew correction, and normalization. Handcrafted features comprising Histogram of Oriented Gradients (HOG), Scale-Invariant Feature Transform (SIFT), and Zernike Moments are extracted to capture structural and shape-based properties. In parallel, spatial and temporal features are learned using a Convolutional Neural Network (CNN) and Long Short-Term Memory (LSTM) architecture. The outputs from the handcrafted and deep-learning pathways are fused to generate a composite feature vector, which is subsequently classified to identify the script or language of the handwritten data. The method provides improved recognition accuracy in the presence of noise, distortions, illumination variations, and inconsistent handwriting styles. The invention is applicable to multilingual handwritten document processing, digitization, and integration with OCR systems.
No. of Pages : 13 No. of Claims : 9

Dr. Navya R, Department of ECE, DSU, secured an Indian patent for “System and Method for Artifact Suppression in Bandwidth-Constrained Wireless Image Transmission using Lightweight Deep Learning and Generative Models,” advancing wireless image quality through lightweight GAN-based artifact suppression.



(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :07/03/2026

(21) Application No.202641026923 A
(43) Publication Date : 20/03/2026

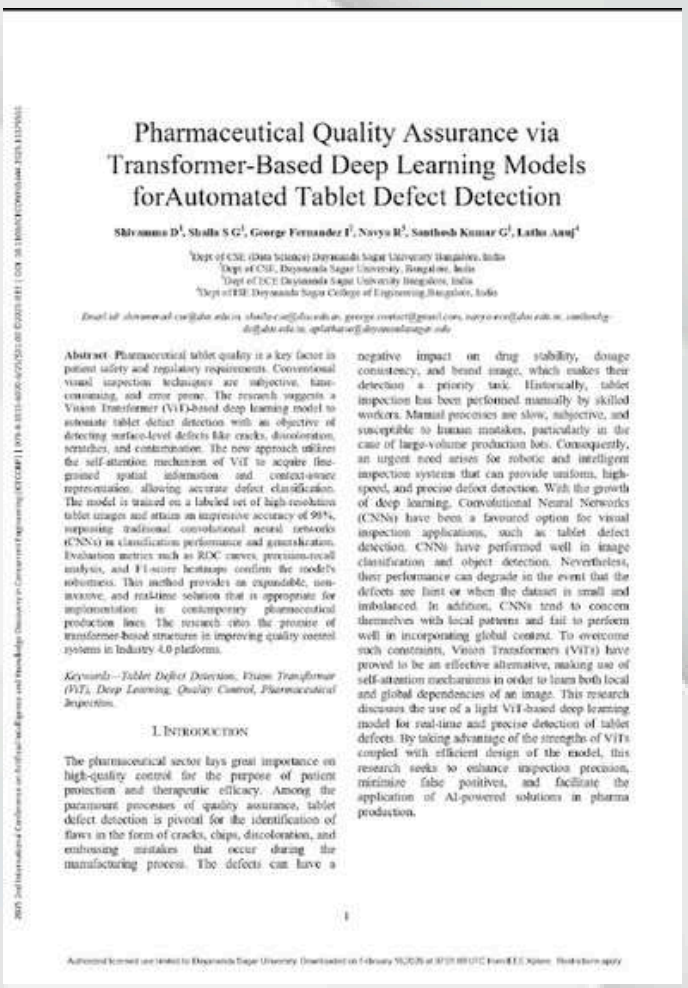
(54) Title of the invention : System and Method for Artifact Suppression in Bandwidth-Constrained Wireless Image Transmission Using Lightweight Deep Learning and Generative Models

(51) International classification :G06N 3/04, G06N 3/08, G06T 5/00, G06V 10/764, 10/82, H04N 19/176
(31) Priority Document No :NA
(32) Priority Date :NA
(33) Name of priority country :NA
(86) International Application No : Filing Date :01/01/1900
(87) International Publication No : NA
(61) Patent of Addition to Application Number :NA Filing Date :NA
(62) Divisional to Application Number :NA Filing Date :NA

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3)Dr. Arun Ananthanarayanan
4)Dr. Santosh Kumar J
5)Dr. Spoorthi B S

(57) Abstract :
Wireless image transmission systems often operate under strict bandwidth limitations and noisy channel conditions, requiring aggressive lossy compression during data transmission. These constraints introduce visual artifacts such as blocking, blurring, and ringing, which significantly degrade image quality and negatively impact downstream computer vision tasks like object recognition and classification. This work presents a deep learning-based framework for suppressing compression and transmission artifacts in bandwidth-constrained wireless imaging environments. The proposed approach integrates a lightweight Generative Adversarial Network (GAN) and a Denoising Convolutional Neural Network (DnCNN) to enhance perceptual image quality at the receiver side. The GAN employs a compact encoder-decoder generator and a shallow discriminator trained using a composite loss function combining adversarial loss, perceptual loss derived from the VGG Network, and the perceptual similarity metric LPIPS (Learned Perceptual Image Patch Similarity). This perceptual training strategy prioritizes visual realism by restoring fine textures and structural details lost during compression. In parallel, the DnCNN model learns a residual mapping to remove compression artifacts and mild channel noise effectively. Extensive experiments conducted in a MATLAB-based simulation framework demonstrate that the proposed methods significantly improve image quality in terms of Structural Similarity Index Measure, Peak Signal-to-Noise Ratio, and Natural Image Quality Evaluator metrics. Furthermore, model optimization techniques including structured pruning and INT8 quantization reduce model size and inference latency, enabling efficient deployment on embedded devices. The restored images also improve the accuracy of downstream vision systems, demonstrating the effectiveness of the proposed framework for practical wireless imaging applications.
No. of Pages : 18 No. of Claims : 8

Dr. Navya R, Department of ECE, DSU, published the IEEE conference paper “Pharmaceutical Quality Assurance via Transformer-Based Deep Learning Models for Automated Tablet Defect Detection” at ICECONF 2025, advancing AI-driven pharmaceutical quality inspection.



Pharmaceutical Quality Assurance via Transformer-Based Deep Learning Models forAutomated Tablet Defect Detection

Shivamma D[1], Shalla S G[2], George Fernander I[3], Navya R[3], Santhosh Kumar G[4], Latha Anuj[4]

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[2]Dept of CSE, Dayananda Sagar University, Bangalore, India
[3]Dept of ECE Dayananda Sagar University Bangalore, India
[4]Dept of ISE Dayananda Sagar College of Engineering,Bangalore, India

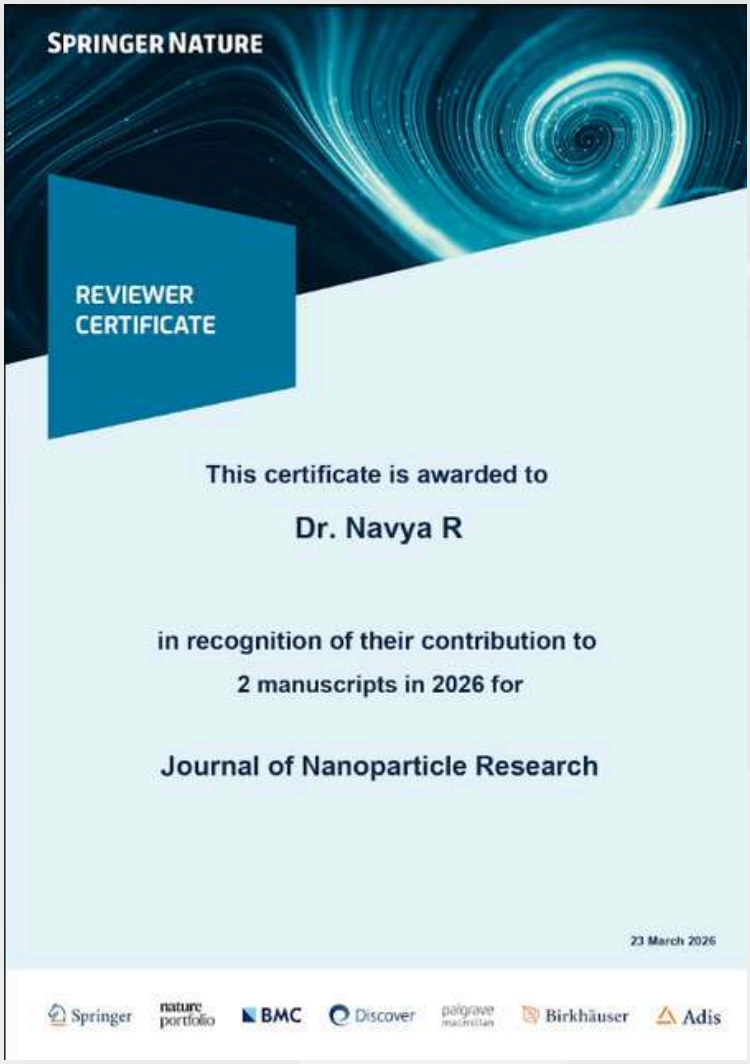
Abstract—Pharmaceutical tablet quality is a key factor in patient safety and regulatory requirements. Conventional visual inspection techniques are subjective, time-consuming, and error prone. The research suggests a Vision Transformer (ViT)-based deep learning model to automate tablet defect detection with an objective of detecting surface-level defects like cracks, discoloration, scratches, and contamination. The new approach utilizes the self-attention mechanism of ViT to acquire fine-grained spatial information and context-aware representation, allowing accurate defect classification. The model is trained on a labeled set of high-resolution tablet images and attains an impressive accuracy of 99%, surpassing traditional convolutional neural networks (CNNs) in classification performance and generalization. Evaluation metrics such as ROC curves, precision-recall analysis, and F1-score heatmaps confirm the model's robustness. This method provides an expandable, non-invasive, and real-time solution that is appropriate for implementation in contemporary pharmaceutical production lines. The research cites the promise of transformer-based structures in improving quality control systems in Industry 4.0 platforms.

Keywords—Tablet Defect Detection, Vision Transformer (ViT), Deep Learning, Quality Control, Pharmaceutical Inspection.

I. Introduction

The pharmaceutical sector lays great importance on high-quality control for the purpose of patient protection and therapeutic efficacy. Among the paramount processes of quality assurance, tablet defect detection is pivotal for the identification of flaws in the form of cracks, chips, discoloration, and embossing mistakes that occur during the manufacturing process. The defects can have a negative impact on drug stability, dosage consistency, and brand image, which makes their detection a priority task. Historically, tablet inspection has been performed manually by skilled workers. Manual processes are slow, subjective, and susceptible to human mistakes, particularly in the case of large-volume production lots. Consequently, an urgent need arises for robotic and intelligent inspection systems that can provide uniform, high-speed, and precise defect detection. With the growth of deep learning, Convolutional Neural Networks (CNNs) have been a favoured option for visual inspection applications, such as tablet defect detection. CNNs have performed well in image classification and object detection. Nevertheless, their performance can degrade in the event that the defects are faint or when the dataset is small and imbalanced. In addition, CNNs tend to concern themselves with local patterns and fail to perform well in incorporating global context. To overcome such constraints, Vision Transformers (ViTs) have proved to be an effective alternative, making use of self-attention mechanisms in order to learn both local and global dependencies of an image. This research discusses the use of a light ViT-based deep learning model for real-time and precise detection of tablet defects. By taking advantage of the strengths of ViTs coupled with efficient design of the model, this research seeks to enhance inspection precision, minimize false positives, and facilitate the application of AI-powered solutions in pharma production.

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Dr. Navya R, has been awarded a Reviewer Certificate by Springer Nature in recognition of reviewing two manuscripts in 2026 for the Journal of Nanoparticle Research, highlighting her contribution to maintaining high standards in research publications.

Dr. Divyashree H B

The research team comprising Dr. Divyashree H B, Dr. Puttamadappa C, Dr. Arun Balodi, Prof. Kokila S, Prof. Jaishree Ramadevaru, and Dr. Supraja Eduru published an Indian patent titled “Real-Time EEG-Based P300 System for Neurocognitive Anomaly Detection in ADHD and Autism” on 20 February 2026. The invention integrates EEG signal processing and machine learning for real-time neurocognitive monitoring and early anomaly detection.



(12) PATENT APPLICATION PUBLICATION (21) Application No.202641012359 A
(19) INDIA
(22) Date of filing of Application :05/02/2026 (43) Publication Date : 20/02/2026

(54) Title of the invention : Real-Time EEG-Based P300 System for Neurocognitive Anomaly Detection in ADHD and Autism

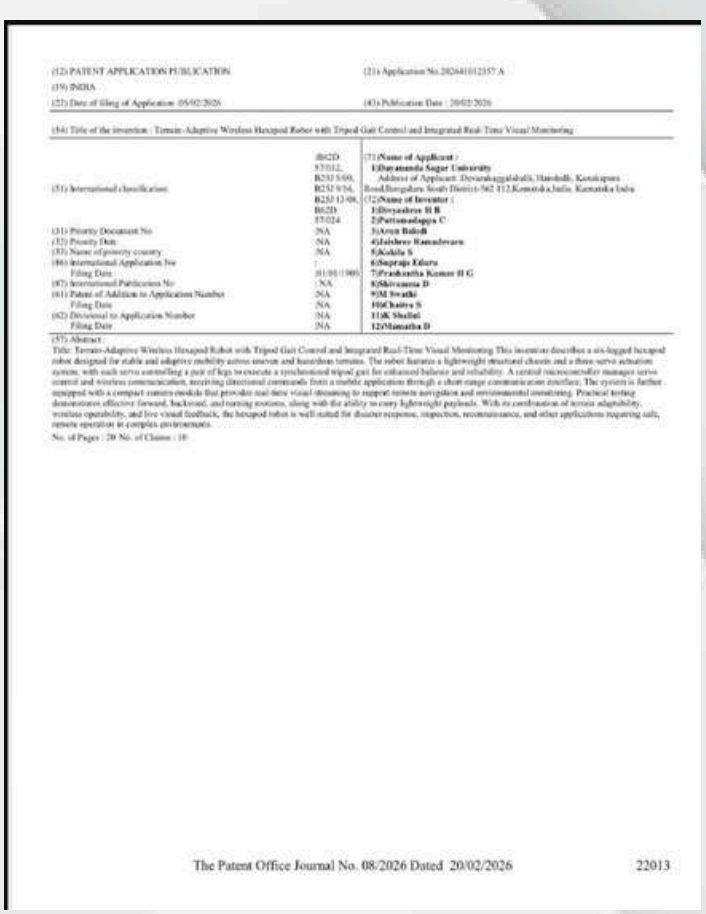
(51) International classification: A61B 5/00, A61B 5/372, A61B 5/16
(31) Priority Document No: NA
(32) Priority Date: NA
(33) Name of priority country: NA
(86) International Application No: Filing Date: 01/01/1900
(87) International Publication No: NA
(61) Patent of Addition to Application Number: NA; Filing Date: NA
(62) Divisional to Application Number: NA; Filing Date: NA

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6)Supraja Eduru
7)Prashantha Kumar H G
8)Shivasmita D
9)Shri S N
10)Dev Sharma

(57) Abstract :
Title: Real-Time EEG-Based P300 System for Neurocognitive Anomaly Detection in ADHD and Autism This technology discloses a real-time neurocognitive anomaly detection system that identifies behavioral and developmental irregularities through the extraction and analysis of the P300 Event-Related Potential from electroencephalography signals. The system integrates a lowcost, high-signal-quality EEG acquisition module with active electrodes, an optimized analog front-end, and a microcontroller-based digitization unit for continuous monitoring. Visual and auditory oddball stimuli are used to evoke P300 responses, which are processed through advanced pre-processing, artifact removal, and discrete wavelet transform–based feature extraction. The system computes P300 amplitude and latency as objective biomarkers and employs machine learning models to classify patterns related to ADHD, ASD, cognitive delay, and sensory overload. Real-time behavioral escalation detection enables early alerts through a connected interface, supporting timely intervention. The technology provides an economical, portable, and clinically useful solution for early neurodevelopmental screening across homes, schools, therapy centers, and low-resource healthcare environments.
No. of Pages : 26 No. of Claims : 10

The Patent Office Journal No. 08/2026 Dated 20/02/2026 22015



(12) PATENT APPLICATION PUBLICATION (21) Application No.202641012357 A
(19) INDIA
(22) Date of filing of Application :05/02/2026 (43) Publication Date : 20/02/2026

(54) Title of the invention : Terrain-Adaptive Wireless Hexapod Robot with Tripod Gait Control and Integrated Real-Time Visual Monitoring

(51) International classification: B62D 57/032, B25J 5/00, B25J 9/16, B25J 13/08, B62D 57/024
(31) Priority Document No: NA
(32) Priority Date: NA
(33) Name of priority country: NA
(86) International Application No: Filing Date: 01/01/1900
(87) International Publication No: NA
(61) Patent of Addition to Application Number: NA; Filing Date: NA
(62) Divisional to Application Number: NA; Filing Date: NA

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6)Supraja Eduru
7)Prashantha Kumar H G
8)Shivasmita D
9)M Swathi
10)Chaitra S
11)K Shalini
12)Samantha D

(57) Abstract :
Title: Terrain-Adaptive Wireless Hexapod Robot with Tripod Gait Control and Integrated Real-Time Visual Monitoring This invention describes a six-legged hexapod robot designed for stable and adaptive mobility across uneven and hazardous terrains. The robot features a lightweight structural chassis and a three-servo actuation system, with each servo controlling a pair of legs to execute a synchronized tripod gait for enhanced balance and reliability. A central microcontroller manages servo control and wireless communication, receiving directional commands from a mobile application through a short-range communication interface. The system is further equipped with a compact camera module that provides real-time visual streaming to support remote navigation and environmental monitoring. Practical testing demonstrates effective forward, backward, and turning motions, along with the ability to carry lightweight payloads. With its combination of terrain adaptability, wireless operability, and live visual feedback, the hexapod robot is well-suited for disaster response, inspection, reconnaissance, and other applications requiring safe, remote operation in complex environments.
No. of Pages : 29 No. of Claims : 10

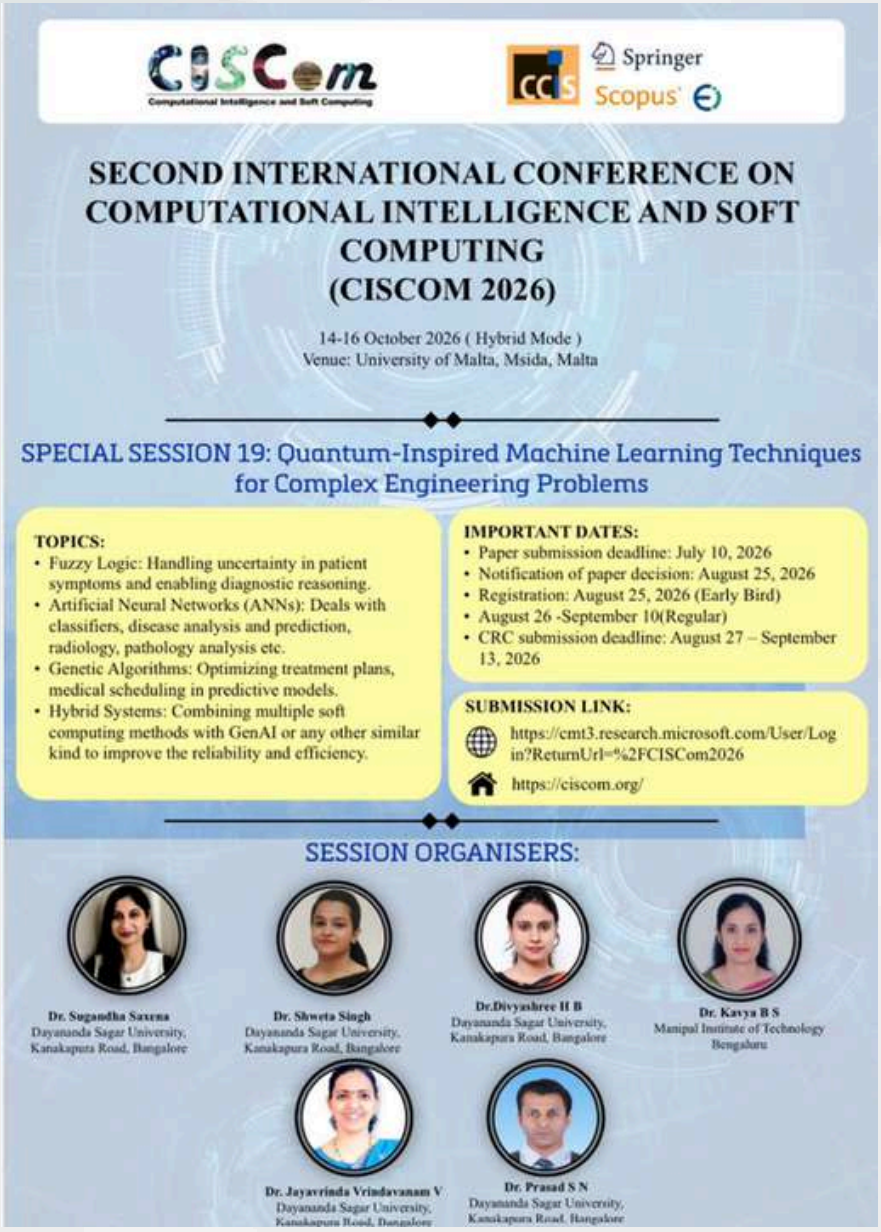
The Patent Office Journal No. 08/2026 Dated 20/02/2026 22013

The research team comprising Dr. Divyashree H B, Dr. Puttamadappa C, Dr. Arun Balodi, Prof. Jaishree Ramadevaru, Prof. Kokila S, and Dr. Supraja Eduru published an Indian patent titled “Terrain-Adaptive Wireless Hexapod Robot with Tripod Gait Control and Integrated Real-Time Visual Monitoring” on 20 February 2026. The innovation enables stable mobility, remote operation, and real-time monitoring across challenging terrains, with applications in disaster response and inspection.

Dr. Divyashree HB, from the Department of Electronics and Communication Engineering, Dayananda Sagar University, received a Certificate of Appreciation for serving as a Reviewer for the International Conference on Computational Intelligence, Data Science and Digital Transformations (ICCISDT-2026). The conference was organized by the Department of Computer Science & Information Technology, School of Technology, Maulana Azad National Urdu University (MANUU), Hyderabad, and was held on 15–16 January 2026. The conference was associated with UPNM, the Ministry of Electronics & Information Technology, Government of India, VYANG Sarthi, and Springer, reflecting its international and academic significance. The certificate recognizes Dr. Divyashree HB's contribution to the peer-review process and her role in supporting the evaluation and quality of research presented at the conference.



Dr. Divyashree H B served as a Session Organizer for Special Session 19, “Quantum-Inspired Machine Learning Techniques for Complex Engineering Problems,” at CISCOM 2026, the Second International Conference on Computational Intelligence and Soft Computing, scheduled for 14–16 October 2026 at the University of Malta, Malta. The session focuses on fuzzy logic, artificial neural networks, genetic algorithms, and hybrid computational methods for addressing complex engineering problems.



Dr. Divyashree H B and co-inventors filed the patent application “System and Method for Voice-Activated Emergency Alerting and Real-Time Location Tracking” under Dayananda Sagar University. Published on 20 February 2026, the invention provides voice-activated emergency alerts, real-time location tracking, and automated response coordination for enhanced personal and women’s safety.



(12) PATENT APPLICATION PUBLICATION (21) Application No.202641012364 A

(19) INDIA

(22) Date of filing of Application :05/02/2026 (43) Publication Date : 20/02/2026

(54) Title of the invention : System and Method for Voice-Activated Emergency Alerting and Real-Time Location Tracking

(51) International classification :H04W 4/90, G08B 25/01, H04W 4/029, H04W 4/02, H04M 11/04

(31) Priority Document No :NA
(32) Priority Date :NA
(33) Name of priority country :NA
(86) International Application No : Filing Date :01/01/1900
(87) International Publication No :NA
(61) Patent of Addition to Application Number :NA Filing Date :NA
(62) Divisional to Application Number :NA Filing Date :NA

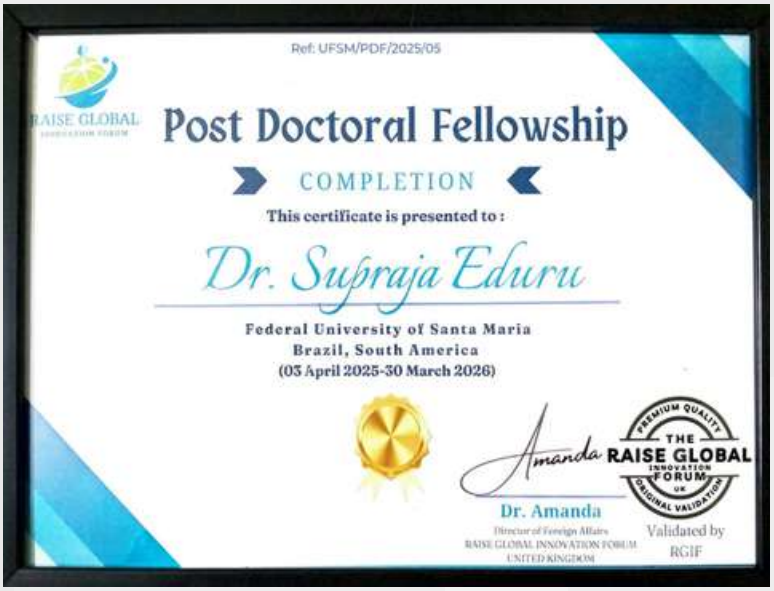
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(72)Name of Inventor :
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7)Prashantha Kumar H G
8)Shivanna D
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11)Vikramadhitya M
12)Sushrutha H K

(57) Abstract :
Title: System and Method for Voice-Activated Emergency Alerting and Real-Time Location Tracking The present disclosure pertains to a voice-activated emergency safety and real-time location tracking system designed to enhance women's personal security during distress situations. The system enables hands-free emergency activation through predefined voice commands, eliminating the need for manual interaction with a device. Upon detecting the distress command, the system automatically triggers an emergency response sequence that includes continuous acquisition of real-time geographic location, transmission of location-based alert messages, and initiation of an automated emergency voice call to registered contacts. Emergency data, including live location and timestamps, is also synchronized with a cloud-based platform to enable remote monitoring and improve response coordination. The system operates reliably in both connected and low-connectivity environments through cellular communication support and incorporates multi-channel alerting to increase notification success. Designed in a compact and portable form, the innovation provides a practical, dependable, and scalable solution for women's safety, as well as broader applications in personal and emergency assistance scenarios.
No. of Pages : 20 No. of Claims : 10

The Patent Office Journal No. 08/2026 Dated 20/02/2026 22017

Dr. Supraja Eduru



Dr. Supraja Eduru successfully completed a Postdoctoral Fellowship at the Federal University of Santa Maria, Brazil, from 3 April 2025 to 30 March 2026, recognized by RGIF, UK, marking a milestone in her research career and international academic collaboration.

Dr. Supraja Eduru, Dr. Divyashree H B, Prof. Jaishree R Devaru, and Prof. Kokila S published an Indian patent titled “Intelligent Traffic Signal Control System and Method for Autonomous Emergency Vehicle Prioritization and Dynamic Green Corridor Generation” on 20 February 2026, advancing intelligent traffic management and emergency vehicle prioritization.



(12) PATENT APPLICATION PUBLICATION
(21) Application No.202641012358 A
(19) INDIA
(22) Date of filing of Application :05/02/2026
(43) Publication Date : 20/02/2026

(54) Title of the invention : Intelligent Traffic Signal Control System and Method for Autonomous Emergency Vehicle Prioritization and Dynamic Green Corridor Generation

(51) International classification : G08G 1/07, G08G 1/08, G08G 1/081, G08G 1/01, G08G 1/087

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(72)Name of Inventor :
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2)Divyashree H B
3)Jaishree R Devaru
4)Kokila S
5)Dev Sharma

(31) Priority Document No :NA
(32) Priority Date :NA
(33) Name of priority country :NA
(86) International Application No Filing Date :01/01/1900
(87) International Publication No :NA
(61) Patent of Addition to Application Number :NA Filing Date :NA
(62) Divisional to Application Number :NA Filing Date :NA

(57) Abstract :
Title: Intelligent Traffic Signal Control System and Method for Autonomous Emergency Vehicle Prioritization and Dynamic Green Corridor Generation An intelligent traffic signaling system is disclosed for autonomously prioritizing ambulances at road intersections by dynamically creating a green corridor without human intervention. The system operates as a standalone unit interfacing directly with existing traffic signal infrastructure and employs one or more complementary emergency vehicle detection mechanisms, including device-enabled transmitter–receiver communication, audio-based siren detection using machine learning classification, and camera-based vision detection. A local controller executes real-time decision logic to override normal traffic signal cycles, selectively granting a green signal to the ambulance approach lane while holding conflicting directions at red, and automatically restoring normal operation after passage. The system supports fallback operation between detection modalities, directional inference to prevent incorrect lane activation, and priority handling for multiple emergency vehicles. By eliminating reliance on GPS, mobile applications, centralized control rooms, and continuous internet connectivity, the invention provides a scalable, cost-effective, privacy-preserving, and reliable solution for reducing ambulance delay and improving emergency response outcomes.
No. of Pages : 21 No. of Claims : 9

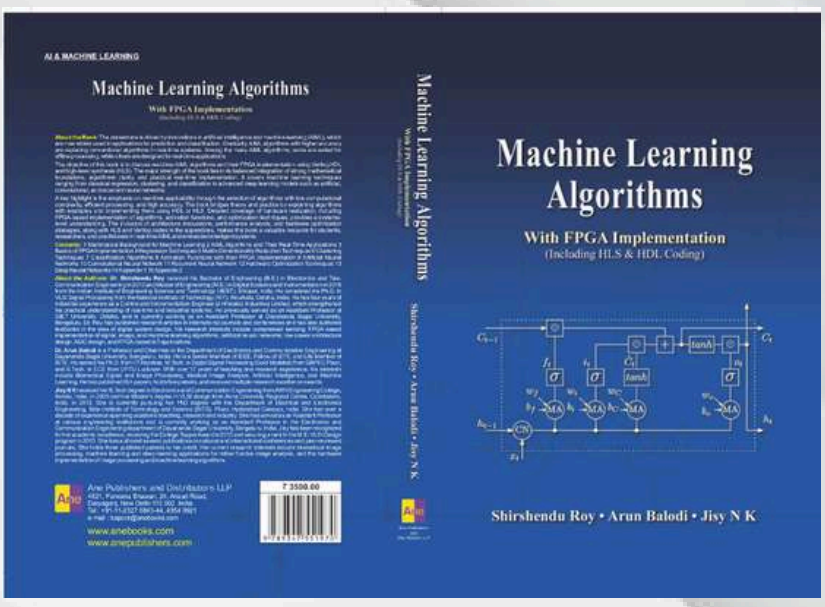
Dr. Shirshendu Roy

Dr. Shirshendu Roy participated in the TechPulse – Early Engagement Program FDP 2026, organized by Tata Technologies, Bengaluru, from 19–23 January 2026, enhancing industry-oriented learning and academia–industry collaboration.



Dr. Shirshendu Roy, Dr. Arun Balodi, and Prof. Jisy N K published the book “Machine Learning Algorithms with FPGA Implementation” with Ane Books Private Ltd. on 20 February 2026. The book covers ML algorithms, AI applications, FPGA programming, neural networks, hardware optimization, and practical HLS/HDL coding examples.

ISBN: 978-93-47551-97-0 | Ane Books





Journal of Embedded & Digital System Design
2025, VOL. 01, NO. 1, 1–10
http://dx.doi.org/xx.xxxx/jeds/XXXXX

A Survey on Different Strategies for Hardware Implementation of Activation Functions

Shirshendu Roy[1] and Jisy N K[1]

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Abstract

Activation functions (AFs) are fundamental components of neural networks (NNs), introducing nonlinearity that enables models to learn complex representations and decision boundaries. With the growing adoption of NNs in real-time and embedded systems, there is an increasing demand for efficient hardware implementations. Implementing AFs on hardware poses significant challenges due to the presence of nonlinear operations and transcendental functions, especially exponential computations required by commonly used AFs such as sigmoid, hyperbolic tangent, and softmax. Efficient approximation and computation techniques for exponential functions (EFs) are essential to enable practical and high-performance hardware realizations of AFs.

This paper presents a comprehensive survey of techniques for implementing AFs on digital hardware. The contributions include a concise review of widely used and emerging AFs, a survey of major EF computation methods such as lookup tables, polynomial and piecewise approximations, COordinate Rotation Digital Compute (CORDIC) based approaches, and iterative algorithms, and a detailed examination of hardware-oriented implementation strategies for AFs. The surveyed techniques are analyzed in terms of accuracy, resource utilization, latency, and power efficiency. This survey aims to provide valuable insights and design guidelines for researchers and practitioners developing efficient NN accelerators on field gate programmable array (FPGA) and other digital hardware platforms.

Keywords: Field Programmable Gate Array (FPGA), Activation Function Architectures, Exponential Function Architectures, Sigmoid Functions, Hyperbolic Tangent.

1 Introduction

Activation functions (AFs) are fundamental components of artificial NNs (ANNs) that introduce nonlinearity into the model. Mathematically, an AF maps the weighted sum of inputs and bias of a neuron to an output signal, thereby determining the activation state of the neuron. Without AFs, a NN would effectively behave as a linear model irrespective of the number of layers, significantly limiting its ability to learn complex patterns.

The output of a neuron in a feedforward ANN is given by

$$\mathbf{a}^{(l+1)} = \phi\left(\mathbf{W}^{(l)}\mathbf{a}^{(l)} + \mathbf{b}^{(l)}\right), \quad (1)$$

where $\mathbf{a}^{(l)}$ and $\mathbf{a}^{(l+1)}$ are input and output activations at layer l and $l+1$ respectively, $\phi(\cdot)$ is the AF, $\mathbf{W}$ is the weight matrix, and $\mathbf{b}$ is the bias vector.

AFs are employed to enable neural networks (NNs) to model complex and nonlinear relationships inherent in real-world data. By introducing nonlinearity, they allow deep networks to approximate arbitrary functions and learn hierarchical feature representations across multiple layers. Furthermore, AFs strongly influence training behavior, including gradient propagation, convergence speed, numerical stability, and susceptibility to issues such as vanishing or exploding gradients. Consequently, the selection of an appropriate AF plays a crucial role in determining network performance, training efficiency, and implementation feasibility.

AFs are used across a wide range of NN architectures and in many machine learning algorithms. They are integral to feedforward NNs, convolutional NNs (CNNs), recurrent NNs (RNNs), transformers, and spiking NNs (SNN). Real-time applications demand for efficient implementation of these networks on digital hardware like field programmable gate array (FPGA). Thus numerous research works have been carried to find efficient techniques to implement the AFs.

Major contributions of this manuscript are

1. All kinds of AFs are briefly discussed.
2. A detailed survey on different techniques to implement exponential function (EF) is presented.
3. Different techniques to implement AFs are discussed in details.

The manuscript is organized in seven sections. Section II discusses about different AFs used in NN architectures. A brief study on techniques to implement EF is discussed in Section III. Section IV discusses about different techniques to implement different AFs. Section V discusses about different estimation metrics and performance analysis of different architectures. Conclusive remarks are made in Section VI.

2 Different Activation Functions

2.1 Binary Activation Functions

Binary AFs limits the output of a node to one of two values. They also called as threshold AFs or Heaviside function. These kind of functions are used in single layer

Dr. Shirshendu Roy and Prof. Jisy N K published “A Survey on Different Strategies for Hardware Implementation of Activation Functions” in the Journal of Embedded and Digital System Design on 29 January 2026, reviewing hardware-based techniques for implementing neural network activation functions.

DOI: 10.5281/zenodo.18397422

Dr. G. Santhosh

Dr. G. Santhosh, Assistant Professor, ECE, DSU, completed the five-day online FDP “Power Quality Challenges and Mitigation Techniques in EV Charging and Renewable-Rich Distribution Systems (EVRD-2026)” from 16–20 February 2026, enhancing his expertise in sustainable power systems and EV charging technologies.


CIN: U80302BR2018PTC038026

Annant Gyan
KNOWLEDGE AND SKILLS PRIVATE LIMITED

Certificate

This is to certify that

DR. G. SANTHOSH

Assistant Professor, ECE, School of Engineering, Dayananda Sagar University, Harohalli, Karnataka
Participated and successfully completed five-days online “Faculty Development Program” on the topic
“Power Quality Challenges and Mitigation Techniques in EV Charging and Renewable-Rich Distribution Systems” [EVRD-2026]
[From 16th February to 20th February 2026]

Date: 27th February 2026

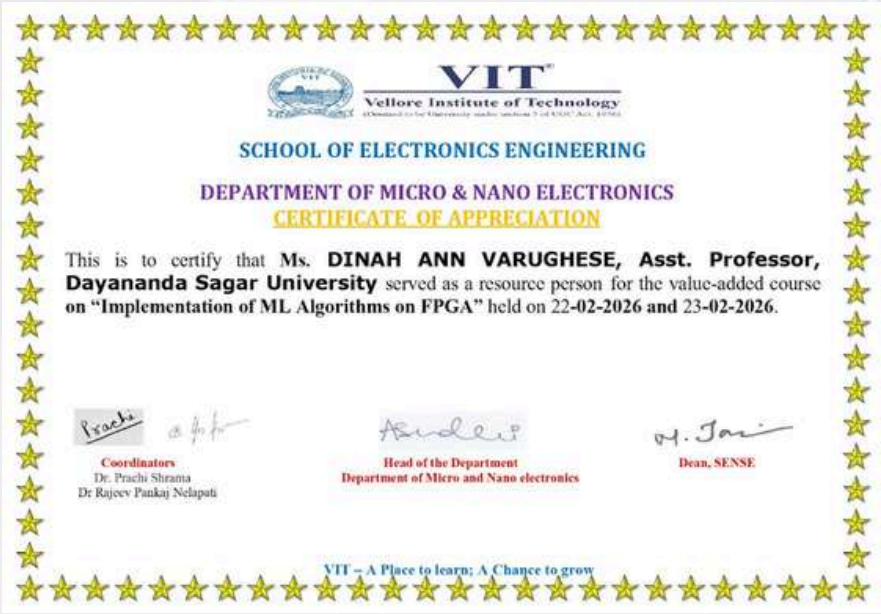
Amar Nath Dubey
Founder & Director

www.annantgyan.com

AGKSPL/SDTP/FDP/EVRD-2026/EVRD-11

Dr. Dinah Ann Varughese

Dr. Dinah Ann Varughese, Assistant Professor, ECE, DSU, served as a Technical Session Resource Person at VIT Vellore for the course “Implementation of ML Algorithms on FPGA” on 22–23 February 2026. Her sessions covered CNNs, hardware-efficient neural networks, BRAM optimization, and model compression, promoting AI hardware acceleration and academic collaboration.


VIT
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SCHOOL OF ELECTRONICS ENGINEERING

DEPARTMENT OF MICRO & NANO ELECTRONICS

CERTIFICATE OF APPRECIATION

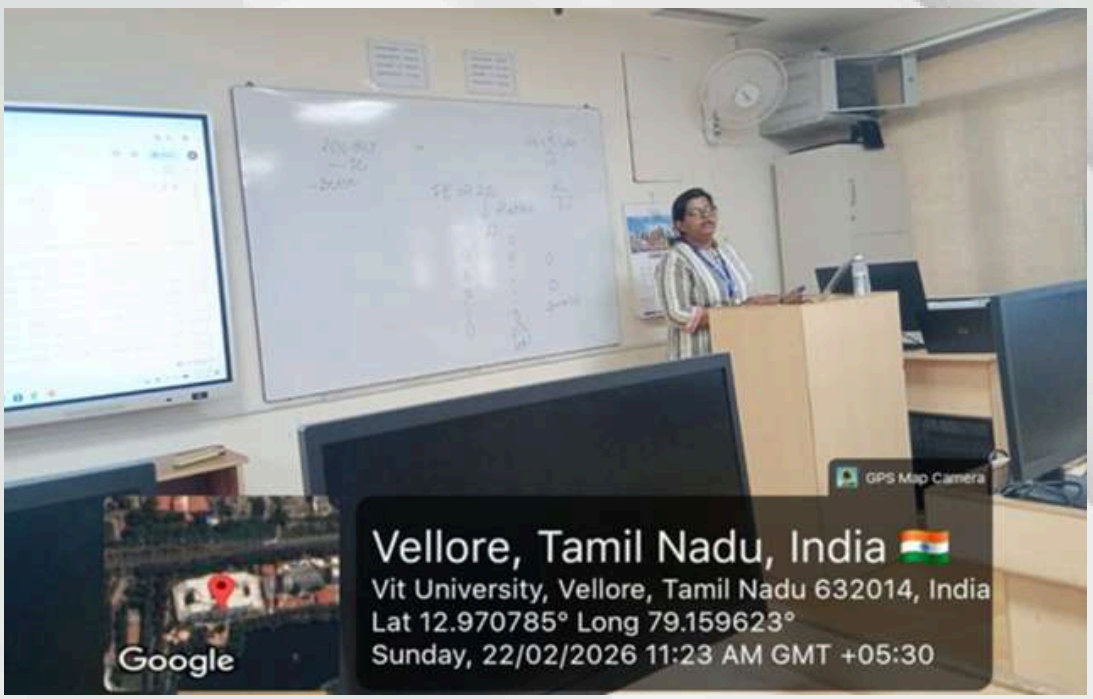
This is to certify that **Ms. DINAH ANN VARUGHESE, Asst. Professor, Dayananda Sagar University** served as a resource person for the value-added course on **“Implementation of ML Algorithms on FPGA”** held on 22-02-2026 and 23-02-2026.

Coordinators
Dr. Prachi Sharma
Dr Rajeev Pankaj Nelapati

Head of the Department
Department of Micro and Nano electronics

Dean, SENSE

VIT – A Place to learn; A Chance to grow



Prof. Dinah Ann Varughese, Assistant Professor, ECE, DSU, published "Synergistic Enhancement of Mechanical and Interfacial Properties in Carbon Fiber Epoxy Nanocomposites via Dual Functionalization of Fiber and Exfoliated Hexagonal Boron Nitride Nanosheets" in Polymer Composites (Wiley, Q1, Impact Factor 4.7). The study used FTIR, XPS, contact angle analysis, and FESEM–EDS to validate hybrid interphase formation, demonstrating improved tensile, flexural, and interlaminar shear properties through enhanced interfacial adhesion and stress transfer.



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RESEARCH ARTICLE

Synergistic Enhancement of Mechanical and Interfacial Properties in Carbon Fiber Epoxy Nanocomposites via Dual Functionalization of Fiber and Exfoliated Hexagonal Boron Nitride Nanosheets

Jerrin Joy Varughese[1,2] | Lince Mathew Thomas[1] | Arun Sam Varghese[1,3] | Dinah Ann Varughese[4,5] | T. P. Sumangala[6] | M. S. Sreekanth[1]

[1]Department of Manufacturing Engineering, School of Mechanical Engineering, Vellore Institute of Technology, Vellore, Tamil Nadu, India | [2]Department of Mechanical Engineering, Providence College of Engineering, APJ Abdul Kalam Technological University, Kerala, India | [3]Department of Mechanical Engineering, Carmel College of Engineering & Technology, APJ Abdul Kalam Technological University, Kerala, India | [4]Department of Electronics and Communication Engineering, School of Engineering, Dayananda Sagar University, Bengaluru, India | [5]Department of Micro & Nanoelectronics, School of Electronics Engineering, Vellore Institute of Technology, Vellore, Tamil Nadu, India | [6]Department of Physics, School of Advanced Sciences, Vellore Institute of Technology, Vellore, Tamil Nadu, India

Correspondence: M. S. Sreekanth (sreekanth.ms@vit.ac.in)

Received: 3 December 2025 | **Revised:** 7 March 2026 | **Accepted:** 8 March 2026

Keywords: 3-aminopropyltriethoxysilane | carbon fiber | hexagonal boron nitride nanosheets | interfacial adhesion | mechanical properties | nanocomposite | surface modification

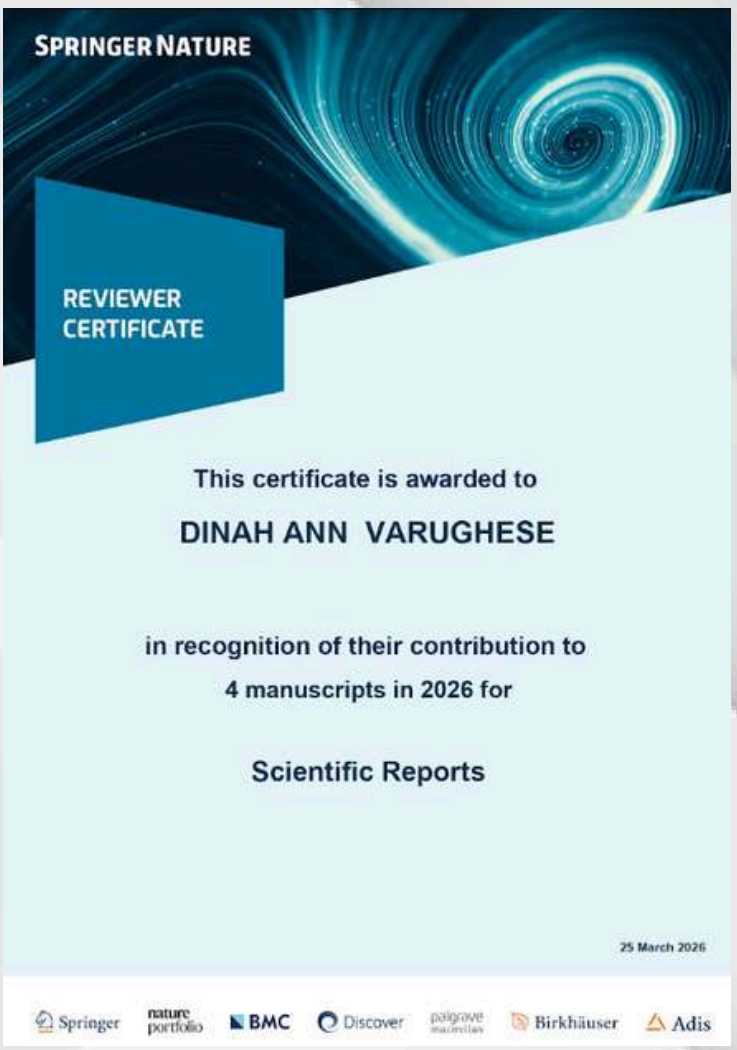
ABSTRACT

A dual interfacial engineering strategy is proposed to enhance the mechanical and interlaminar performance of carbon fiber (CF)-reinforced epoxy (EP) nanocomposites by simultaneously silanizing CF and exfoliated hexagonal boron nitride nanosheets (hBNNs). Sodium hydroxide assisted hydroxylation, followed by 3-aminopropyltriethoxysilane (APTES) functionalization, enabled covalent integration at the fiber–matrix and filler–matrix interfaces. XPS analysis confirmed the formation of Si—O—Si and Si—O—B linkages on APTES functionalized hBNNs, establishing a chemically interconnected interface. Wettability

Prof. Dinah Ann Varughese, Assistant Professor, ECE, DSU, reviewed four manuscripts for Scientific Reports (Springer Nature) in 2026, contributing to the evaluation of AI research involving deep learning-based classification and segmentation.







Dr. Dinah Ann Varughese, Assistant Professor, ECE, DSU, successfully defended her Ph.D. thesis on AI-based edge computing for early cancer cell prediction at VIT Vellore on 19 June 2026. Her research achievements include the VIT Seed Grant, two Raman Research Awards, and the Dr. A.P.J. Abdul Kalam Award.

Prof. Kanmani B S

Prof. Kanmani B S, Assistant Professor, ECE, DSU, participated in the International Congress on Industry 5.0: Human-Centric and Sustainable Development, held on 6–7 February 2026 at Dayananda Sagar College of Engineering, focusing on innovation, sustainability, and human-centered technology.



PARTICIPATION

CERTIFICATE

This certificate is to certify that

Kanmani B S

has actively participated in the International Congress on Industry 5.0: Human-Centric and Sustainable Development on 6th and 7th February, 2026 organized by Department of Computer Science and Engineering at Dayananda Sagar College of Engineering.

Your presence and engagement contributed significantly to the success of this global platform dedicated to fostering innovation, sustainability, and human-centered technological advancement under the vision of Industry 5.0.

We sincerely appreciate your enthusiasm, thoughtful participation, and commitment towards building a future driven by responsible innovation and sustainable growth.

With heartfelt thanks and warm regards.

Dr. D R Ramesh Babu
Vice Principal and Head
Dept. of CSE, DSCE

Dr. Abhinav Karan

Mr. Abhinav Karan participated in the “TechPulse – Early Engagement Program” FDP 2026, organized by Tata Technologies, Bengaluru, from 19 to 23 January 2026. The program focused on industry-oriented learning and early engagement initiatives, strengthening academia–industry collaboration and enhancing professional competencies aligned with current technological practices.



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is awarded to

Mr. Abhinav Karan

in recognition of the active participation in “TechPulse – Early Engagement Program” FDP 2026, organized during 19th January 2026 to 23rd January 2026 at Tata Technologies, Bangalore

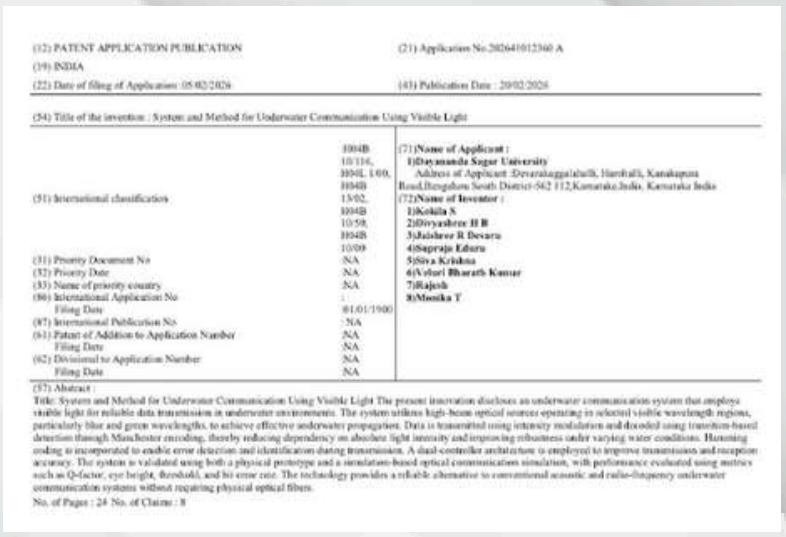
Chief Human Resources Officer

Date : 23rd January 2026

/// Engineering a better world

Prof. Kokila S

Prof. Kokila S, Dr. Divyashree H B, Prof. Jaishree R Devaru, and Dr. Supraja Eduru published the patent “System and Method for Underwater Communication Using Visible Light” in the Indian Patent Office Journal on 20 February 2026, under DSU. The invention uses visible-light technology for reliable underwater data transmission. Captured images are included as evidence.



(12) PATENT APPLICATION PUBLICATION (21) Application No.202641012360 A
(19) INDIA
(22) Date of filing of Application :05/02/2026 (43) Publication Date : 20/02/2026

(54) Title of the invention : System and Method for Underwater Communication Using Visible Light

(51) International classification: H04B 10/116, H04L 1/00, H04B 13/02, H04B 10/58, H04B 10/09

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7)Rajesh
8)Monika T

(31) Priority Document No : NA
(32) Priority Date : NA
(33) Name of priority country : NA
(86) International Application No : NA
Filing Date : 01/01/1900
(87) International Publication No : NA
(61) Patent of Addition to Application Number : NA
Filing Date : NA
(62) Divisional to Application Number : NA
Filing Date : NA

(57) Abstract :
Title: System and Method for Underwater Communication Using Visible Light The present innovation discloses an underwater communication system that employs visible light for reliable data transmission in underwater environments. The system utilizes high-beam optical sources operating in selected visible wavelength regions, particularly blue and green wavelengths, to achieve effective underwater propagation. Data is transmitted using intensity modulation and decoded using transition-based detection through Manchester encoding, thereby reducing dependency on absolute light intensity and improving robustness under varying water conditions. Hamming coding is incorporated to enable error detection and identification during transmission. A dual-controller architecture is employed to improve transmission and reception accuracy. The system is validated using both a physical prototype and a simulation-based optical communication simulation, with performance evaluated using metrics such as Q-factor, eye height, threshold, and bit error rate. The technology provides a reliable alternative to conventional acoustic and radio-frequency underwater communication systems without requiring physical optical fibers.
No. of Pages : 24 No. of Claims : 8

Prof. Jaishree R Devaru



(12) PATENT APPLICATION PUBLICATION (21) Application No.202641012365 A
(19) INDIA
(22) Date of filing of Application :05/02/2026 (43) Publication Date : 20/02/2026

(54) Title of the invention : System and Method for Intelligent Crop Disease Detection, Prediction, and Proactive Treatment

(51) International classification: G06V 10/764, G06V 20/10, G06V 10/774, G06K 9/62, G06V 10/82

(71)Name of Applicant :
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(72)Name of Inventor :
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3)Kokila S
4)Supraja Eduru
5)Shankar N
6)Kishan M
7)Madhuri V
8)Mallikarjun T D

(31) Priority Document No : NA
(32) Priority Date : NA
(33) Name of priority country : NA
(86) International Application No : NA
Filing Date : 01/01/1900
(87) International Publication No : NA
(61) Patent of Addition to Application Number : NA
Filing Date : NA
(62) Divisional to Application Number : NA
Filing Date : NA

(57) Abstract :
Title: System and Method for Intelligent Crop Disease Detection, Prediction, and Proactive Treatment The present disclosure pertains to a smart agriculture system for real-time crop disease detection, forecasting, and treatment guidance, with specific application to tomato plants. The system integrates environmental sensing and leaf image analysis using a hybrid quantum- classical machine learning framework to improve accuracy and robustness under real-field conditions. Distributed sensor nodes collect temperature, humidity, soil moisture, and light intensity data, while a vision-based classifier analyses leaf images captured by a mobile platform. Sensor-based inference and image-based classifications are fused to enable reliable disease identification even with limited agricultural datasets. The disclosure further incorporates a disease forecasting module that predicts disease risk within a four-to-seven-day window, enabling proactive intervention. Upon detection, the system generates farmer-friendly treatment guidance through machine-readable code- based cards and on-device assistance. Designed for real-time, offline field deployment, the technology supports scalable precision agriculture and improved crop health management.
No. of Pages : 25 No. of Claims : 8

Prof. Jaishree R Devaru, Dr. Divyashree H B, Prof. Kokila S, and Dr. Supraja Eduru have successfully published a patent titled “System and Method for Intelligent Crop Disease Detection, Prediction, and Proactive Treatment” in the Indian Patent Office Journal on 20 February 2026.

This work focuses on smart agriculture using machine learning and sensor-based technologies for real-time crop disease detection and management. The department congratulates the authors on this achievement.

Prof. Jisy N K

Prof. Jisy N K presented the paper “Voice and Gesture-Controlled File Management Using Computer Vision” at the 7th International Conference on Mobile Computing and Sustainable Informatics (ICMCSI-2025), organized by Purbanchal University, Nepal, on 7–9 January 2026. The paper was co-authored with Sivasankari S S, K Ganesh Koushik, K Chakridhar Reddy, Indra Kaarthikeya C H, and N Vardhan Reddy.





Dr. Jisy N K successfully defended her Ph.D. on 7 April 2026 at BITS Pilani, Hyderabad Campus. Her thesis focused on explainable deep learning for glaucoma detection using fundus images, resulting in Q1 and Q2 journal publications and international conference presentations. Her research was conducted under the supervision of Prof. Sudha Radhika and Prof. M B Srinivas.

Publications

NAME	PAPER DETAILS
Dr. Arun Balodi	• Clustering-cum-regression based model and performance analysis for early prediction of heart disease • An attention-based multimodal deep learning framework integrating EEG and ECG for enhanced stress detection • An adaptive multiscale local mesh ternary pattern technique with extensive pre-processing and Grey Wolf optimisation based classifiers for oral cancer image classification • Synthetic Aperture Radar Polarimetry for Disaster Analysis • An Analysis of Gaming Devices Adoption among Adults using a Topic Modelling Approach
Dr. S N Prasad	• Mitigating the Threat of DDoS Attacks: Emerging Strategies and Algorithms • Revolutionizing Diabetes Prediction: A Machine Learning Approach to Early Detection and Intervention
Dr. S. Arungalai Vendan	• Statistical Evaluation of Ultrasonic Welding Parameters for PEEK Polymer Using Pearson Heat Map
Dr. Theodore Chandra S	• Statistical Evaluation of Ultrasonic Welding Parameters for PEEK Polymer Using Pearson Heat Map • Benchmarking YOLO Variants on an Unseen Video: A Comparison of Inference Speed, GFLOPs, and Recall
Dr. Gayathri K M	• A 10-bit 45.5-MS/s Asynchronous SAR ADC with a DCDAC Switching Technique in 45nm CMOS • Design and Simulation of a FinFET-Based 11T Schmitt Trigger SRAM Cell Using Cadence • Next Generation Quantum-IoT Communication Framework for Intelligent and Sustainable Network Solutions
Dr. BM Ashwin Desai	• Biomedical Applications and Toxicity Mitigation of Functional Quantum Dots • Nanonizing bioactives: precision chemistry for next-gen therapeutics • Predicting Endocrine Disruptors: A Deep Learning QSAR Model for Estrogen Receptor Activity • Fiber gun: A Portable Nanofiber Delivery System for Accelerated Wound Healing
Dr. Vinu R	• Machine Learning-based Early Diagnosis and EMG-Assisted Monitoring of Parkinson's Disorder • An Integrated Sensor-Based Machine Learning System for Predicting Crops and Fertilizers • Virtual and Soft Sensors for Indoor Air Quality: AI-Driven Architectures, Modelling Techniques, and Future Research Trends • Design and Development of an Optical Sensing System for Palm Based Shear Force Detection • Optimized FBG-Based Vibration Monitoring Using Cantilever for a Rail Wheel Lab Rig Model • A Digital Twin-Enabled Framework for Critical Health Monitoring using Wireless Sensor Networks and Machine Learning

Publications

NAME	PAPER DETAILS
Dr. Arun Ananthanarayanan	• Experimental and Statistical Approach to the Evaluation of Chill Cast LM13/Zircon/Carbon Hybrid Composites' Wear Characteristics • Experimental and machine learning-based analysis of wear behaviour in CNT and titanium reinforced copper matrix composites • Optimized wear behavior of LM13/ zircon/carbon hybrid composites: experimental analysis, statistical modeling, and machine learning predictions
Dr. Sneha Sharma	• Recent Advancements and Emerging Trends in Biosensors: A Review on Disease Diagnosis and Personalized Medicine • Supercontinuum light source for optical coherence tomography using liquid-filled photonic crystal fiber • Design of Strain Monitoring for Wheel Using the Optical Sensor in the Roadway Safety System • Data Extraction and Preprocessing in Residual Recurrent Convolutional Network (RRCN) for Video Super Resolution • Comparative Study of 1-D and 2-D Photonic Crystal Based Biosensor for Detection of Plasmodium Parasite in Cells
Dr. Owais Ahmad Shah	• Enhancing Workability Prediction of Concrete Using Ensemble Machine Learning Models • A CNTFET based process variation resilient SRAM design for stable low power and half select free operation • Data-Driven Prediction of Compressive Strength in High-Performance Concrete • Real-Time Speech Translation for Mobile Communication Using AI-Based Text Recognition • Enhancing JSEG Color Texture Segmentation Using Quaternion Algebra Method • Design and Development of ALU using Multi ChipletMethodologyfor High-Performance Computing
Dr. Godfrey D	• Diabetes Risk Prediction Using Stacked RF and SVM ML Models with SHAP and LIME Interpretability • Next-Gen Solar Tracking for Real-Time Energy Harvesting
Dr. Navya R	• Pharmaceutical Quality Assurance via Transformer-Based Deep Learning Models Forautomated Tablet Defect Detection

Publications

NAME	PAPER DETAILS
Dr. Divyashree H B	• Robotic Operating System-Based Ground Control Station for Unmanned Aerial Vehicles. • An Efficient Smart Agriculture Monitor System Using IoT. • QOS Aware Secure Cluster-Based Routing for Wireless Sensor Networks Using a Multi-Objective-Trust Centric Artificial Algae Algorithm.
Dr. Supraja Eduru	• Design of Health-Aware Assist Smart Trolley Using Low Energy Bluetooth Module • Wireless Data Acquisition Systems for Biomedical Equipment
Dr. Rashmita Sahoo	• PCB Defect Detection by Using Deep Learning Algorithm
Dr. Deepthi Chamkur V	• AI-Driven Mortality Risk Classification Using HMIS Data: A Case Study from Nagaon District, Assam, India
Dr. G Santhosh	• Real-Time Public Transport Tracking for Small Cities: An IoT and AI-based Approach • Serpent-ID: A Deep Learning-Based Mobile Application for Rapid Snake Identification and Bite Management Guidance
Dr. Dasari Srikanya	• Dielectric-Modulated Zinc-Oxide Nanostructured Thin Film Field Effect Transistor
Dr. Ramesh Amugothu	• Compact Ultrawideband Metamaterial Absorber for Triple-Band EMC and EMI Applications • Ultra-Compact Multiband Metasurface Absorber Enabling Advanced Healthcare Sensing Applications
Dr. Dinah Ann Varughese	• Synergistic Enhancement of Mechanical and Interfacial Properties in Carbon Fiber Epoxy Nanocomposites via Dual Functionalization of Fiber and Exfoliated Hexagonal Boron Nitride Nanosheets • FPGA-Accelerated Convolutional Feature Extractor for Real-Time Skin Image Analysis using Optimized Hardware CNN Blocks
Mrs. Kanmani B S	• Diabetes Risk Prediction Using Stacked RF and SVM ML Models with SHAP and LIME Interpretability
Mr. Abhinav Karan	• LangChain Orchestrated Ecosystem for Token-Aware LLM Routing, Hybrid Semantic Retrieval and Explainable Conversational Automation with Dynamic Data Handling

Publications

NAME	PAPER DETAILS
Mr. Nadeem Pasha	• Synergistic role of S-Glass and graphene on the wear performance of Al6061: experimental study and explainable machine learning analysis • Fabrication of highly conductive PEDOT:PSS/CdFe2O4 composite thin films-based sensors towards detection of greenhouse methane gas at ppb level
Mr. V Sudharsan	• Smart Classroom and Timetable Scheduling System using Hybrid Graph Coloring and Cloud Optimization • Real-Time Public Transport Tracking for Small Cities: An IoT and AI-based Approach • Serpent-ID: A Deep Learning-Based Mobile Application for Rapid Snake Identification and Bite Management Guidance • Intelligent Cost Governance in Projects
Mrs. Prabavathi	• Experimental Benchmarking: CAN and I2C Protocols for EV BMS Communication

Students Achievements

Students of the Electronics and Communication Engineering (ECE) program at Dayananda Sagar University, Bengaluru from the 2026 graduating batch have secured placements with Ascent Circuits, where Usha D K (USN: ENG22EC0074) and Sneha V Biradar (USN: ENG22EC0064) received offers with a CTC of ₹6 LPA along with a ₹12,000 stipend, reflecting their strong technical competence and the university's focused training and placement efforts.



SCHOOL OF ENGINEERING

Training & Placement Cell

DSU /Placement /25-26/94 Date: 21-01-2026

Congratulations

Final Selected Students List – 2026 Batch

We are delighted to announce that the following student **have been placed in**

"Ascent Circuits"

Sl No	USN	Name of the Candidate	CTC offered	Branch
1	ENG22EC0074	Usha D K	6 LPA & 12,000 Stipend	ECE
2	ENG22EC0064	Sneha v Biradar	6 LPA & 12,000 Stipend	ECE
3	ENG22DS0010	R SINDHU	6 LPA & 12,000 Stipend	Data Science

M N Guruvenkatesh
Sr. Vice President - Placements & Skill Development
Dayananda Sagar Institutions

Vijay Kumar S
Director - Training & Corporate Relations
Dayananda Sagar University

Rohan Raj (USN: ENG23EC1002), a student of the Electronics and Communication Engineering (ECE) program, Dayananda Sagar University, Bengaluru, has been successfully placed with Taste of Mom as part of the 2026 graduating batch. The offer includes a CTC of ₹4.5 LPA along with a stipend of ₹20,000, reflecting the student's academic performance and employability skills



DAYANANDA SAGAR UNIVERSITY

SCHOOL OF ENGINEERING

Training & Placement Cell

DSU /Placement /25-26/91 Date: 13-01-2026

Congratulations

Final Selected Students List – 2026 Batch

We are delighted to announce that the following student **have been placed in**

"TASTE OF MOM"

Sl No	USN	Name of the Candidate	CTC Offered	Branch
1	ENG22CS0310	Gudivada Pardha	4.5 LPA & 20,000 Stipend	CSE
2	ENG23EC1002	ROHAN RAJ	4.5 LPA & 20,000 Stipend	ECE

M N Guruvenkatesh
Sr. Vice President - Placements & Skill Development
Dayananda Sagar Institutions

Vijay Kumar S
Director - Training & Corporate Relations
Dayananda Sagar University

A paper titled “PCB Defect Detection by Using Deep Learning Algorithm” was presented at the 2025 IEEE North Karnataka Subsection Flagship International Conference (NKCon) by Walter Wellington C (ENG21EC0007), Ankit Shivakumar Hosamani (ENG21EC0024), Chirag D Acharya (ENG21EC0029), and Dhanush K N (ENG21EC0146), students of the Department of ECE, Dayananda Sagar University, under the guidance of Ms. Rashmitha Sahoo, Assistant Professor, ECE.

The team proposed a deep learning–based fusion model combining YOLOv8 and DenseNet for accurate PCB defect detection. The model achieved an impressive 96.5% accuracy, outperforming individual models.

This achievement highlights the department’s strong focus on research, innovation, and practical applications of AI in electronics manufacturing.



2025 IEEE North Karnataka Subsection Flagship International Conference (NKCon)

PCB DEFECT DETECTION BY USING DEEP LEARNING ALGORITHM

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***Abstract*— Traditional PCB defect detection methods, such as manual inspection and rule-based Automatic Optical Inspection (AOI), are increasingly inadequate due to their sensitivity to lighting conditions, alignment issues, and limited scalability. The traditional inspection methods are replaced by various deep learning model (YOLO8 and DenseNet). To improve the accuracy, this study utilizes novel fusion model of YOLO8 (You Only Look Once) object detection algorithm in conjunction with Convolutional Neural Networks (CNNs) to identify various PCB defects, including missing holes, mouse bites, open circuits, short circuits, spurs, and spurious copper. A custom dataset was created using KiCAD generated PCB designs and augmented through flipping, rotation, and tensor-based techniques to enhance model generalization. The model is noble fusion model accuracy is compared with the accuracy of YOLO8 and DenseNet models. The simulation results demonstrate that the accuracy is 96.5%, 91.3% and 86.1% for novel fusion model, YOLO8 and DenseNet respectively. The accuracy of the fusion model (YOLO8+DenseNet) is improved compare to existing models. The proposed model offers a robust, effieient, and scalable solution that reduces the limitations of the exiting models and enhances overall manufacturing reliability.**

Keywords*— *PCB Defect Detection, Deep Learning, YOLO, Convolutional Neural Network (CNN), Automated Optical Inspection (AOI)

I. Introduction

Printed Circuit Boards (PCBs) are fundamental components in almost all electronic devices, acting as the backbone for electrical connectivity among various components such as resistors, capacitors, microcontrollers, and integrated circuits. The increasing complexity and miniaturization of PCBs in industries such as consumer electronics, automotive, aerospace, and medical devices have significantly elevated the need for precise and reliable defect detection during the manufacturing process. Even minor defects such as open circuits, short circuits, missing holes, mouse bites, spurs, or spurious copper can lead to complete functional failure of the final product. Traditionally, PCB defect detection relies on manual inspection or rule-based Automated Optical Inspection (AOI) systems [1]. However, these approaches are limited in accuracy, scalability, and adaptability to varying production environments. Manual inspection is prone to human error and fatigue, while conventional AOI systems struggle under inconsistent lighting, misalignments, and variations in PCB layouts [2]. To overcome the limitation associated with manual and automated optical inspection methods, several studies use machine learning techniques to detect fault in the printed PCB board [3]. Though there are several deep learning-based PCB board fault detection methods, CNN and YOLO provide better results in PCB board fault detection [4]. Till date, no work is devoted to analyze the performance of the PCB board fault detection using the both the CNN and YOLO object detection algorithm. Unlike prior works, this study combines YOLOv8 and DenseNet into a fusion model for higher defect detection accuracy across multiple defect types. This paper proposes a deep learning-based detection system leveraging state-of-the-art Convolutional Neural Networks (CNNs) and the YOLO (You Only Look Once) object detection algorithm. These models are capable of learning intricate patterns from large datasets, allowing for robust, real-time identification of diverse defect types in PCB images. A custom dataset was generated using KiCAD and enhanced through data augmentation techniques such as flipping, rotation, and image transformations to ensure model generalization across different defect scenarios.

This work aims to deliver a scalable and highly accurate defect detection system that minimizes reliance on human expertise, reduces production downtime, and enhances quality assurance in modern PCB manufacturing.

II. Literature Survey

Now-a-days the PCB board fault detection using machine is off high demand due to several benefits such as minimum inspection time, improve accuracy and reliable product with high standard and efficiency. There are several studies which uses different deep learning algorithms and shown the better performance of PCB board fault detection [6]. A comprehensive study by Xing Chen et al. provides a detailed analysis of deep learning-based PCB defect detection techniques, emphasizing the need for robust datasets and well-defined evaluation metrics. The authors review commonly used datasets and algorithms, highlighting challenges in real-world implementations and offering direction for future research in algorithmic enhancement and improved detection accuracy in complex manufacturing environments [7]. Wenbin Chen et al. proposed a defect detection model based on the fusion of multi-scale features and an Efficient Channel Attention Mechanism (ECA-Net). Their model, MSF-ECANet, enhances the weighting of foreground and background channels, resulting in improved object localization and classification performance. The method significantly outperforms traditional detection models in both accuracy and speed, making it well-suited for

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SL. NO	USN	NAME	COMPANY NAME	CTC (LPA)
1	ENG22EC0028	Latheshwar Reddy G B	Adyapan	8
2	ENG22EC0034	Mamatha Bai	Averixis	8
3	ENG22EC0094	S.Sai Giri Charan	Averixis	8
4	ENG22EC0074	Usha D K	EY	6.49
5	ENG22EC0064	Sneha v Biradar	Ascent Circuits	6
6	ENG23EC1007	SONAM	Ericsson	6
7	ENG22EC0001	Aarthi Nayak Ullal	Intrainz	6
8	ENG22EC0036	Mohammed Fazil T M	Exotel	6
9	ENG22EC0028	Latheshwar Reddy G B	Elytespark	6
10	ENG22EC0048	Rakshitha H P	SkillOrbit	6
11	ENG22EC0073	Usha D	SIEMENS	5
12	ENG22EC0026	Kavya S	SIEMENS	5
13	ENG23EC1002	ROHAN RAJ	K12 Techno Services	5
14	ENG22EC0013	CHARAN S	Onepaper Research	4.94
15	ENG23EC1008	Harsha V P	Rinex Technology	4.8
16	ENG22EC0078	varun y	High-Technext	4.75

Placements

SL. NO	USN	NAME	COMPANY NAME	CTC (LPA)
17	ENG23EC1002	ROHAN RAJ	TASTEOFMOM	4.5
18	ENG22EC0005	Ajay S	Skillovilla	4.5
19	ENG22EC0032	Madhu G M	Zepto	4.5
20	ENG22EC0004	Aditya Singh Thakur	Blinkit	4.2
21	ENG22EC0059	Shradha Patil	Yokogova india Pvt Ltd	4.6
22	ENG22EC0066	Supritha B M	Zetwerk Electronics	4
23	ENG22EC0073	Usha D	Zetwerk Electronics	4
24	ENG22EC0107	Sripriya B S	Zetwerk Electronics	4
25	ENG22EC0001	Aarthi Nayak Ullal	Corizo's	4
26	ENG22EC0007	Anusha BM	Corizo's	4
27	ENG22EC0094	S.Sai Giri Charan	Aenexz	4
28	ENG22EC0089	JP HariKrishna Raj	Aenexz	4
29	ENG22EC0007	Anusha BM	Vedupskilling	4
30	ENG22EC0040	Mythri B R	CGI	3.75
31	ENG22EC0096	Surya Narayana Reddy S	Sika Interplant	3
32	ENG22EC0078	varun y	Semperonic	3
33	ENG22EC0082	Vinod Ganiger	Biocon	3

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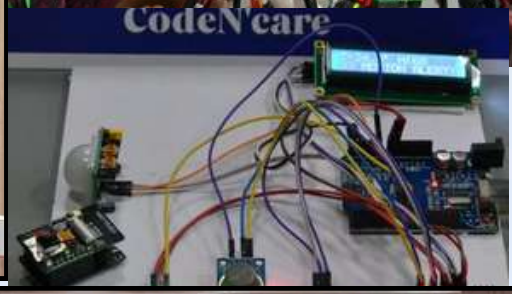
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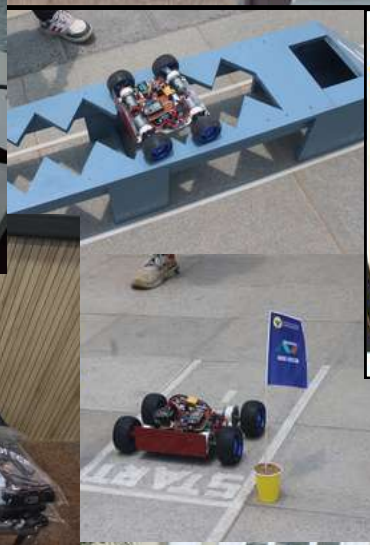



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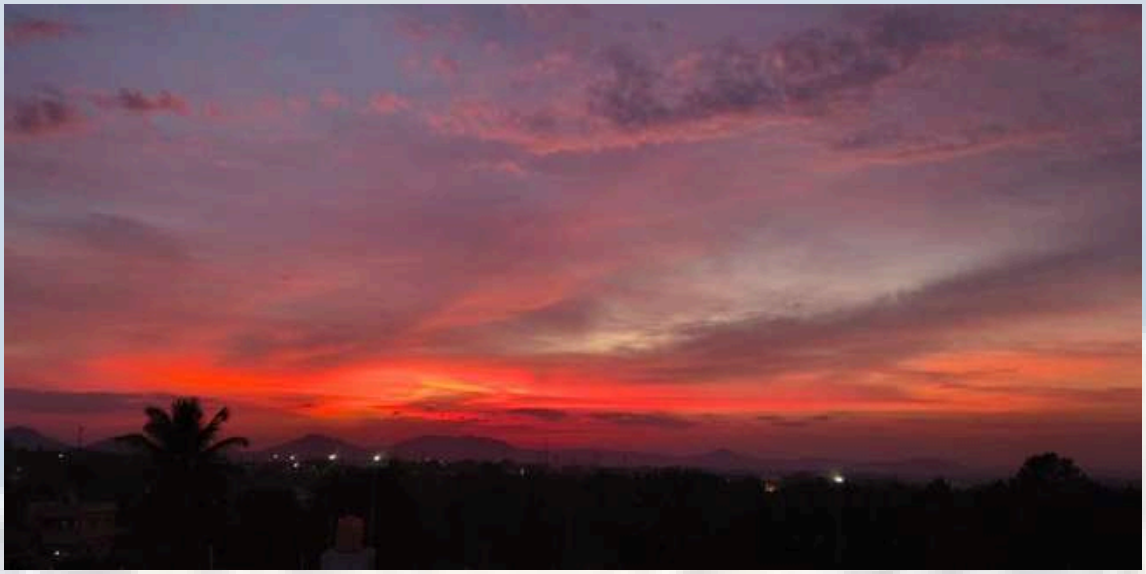


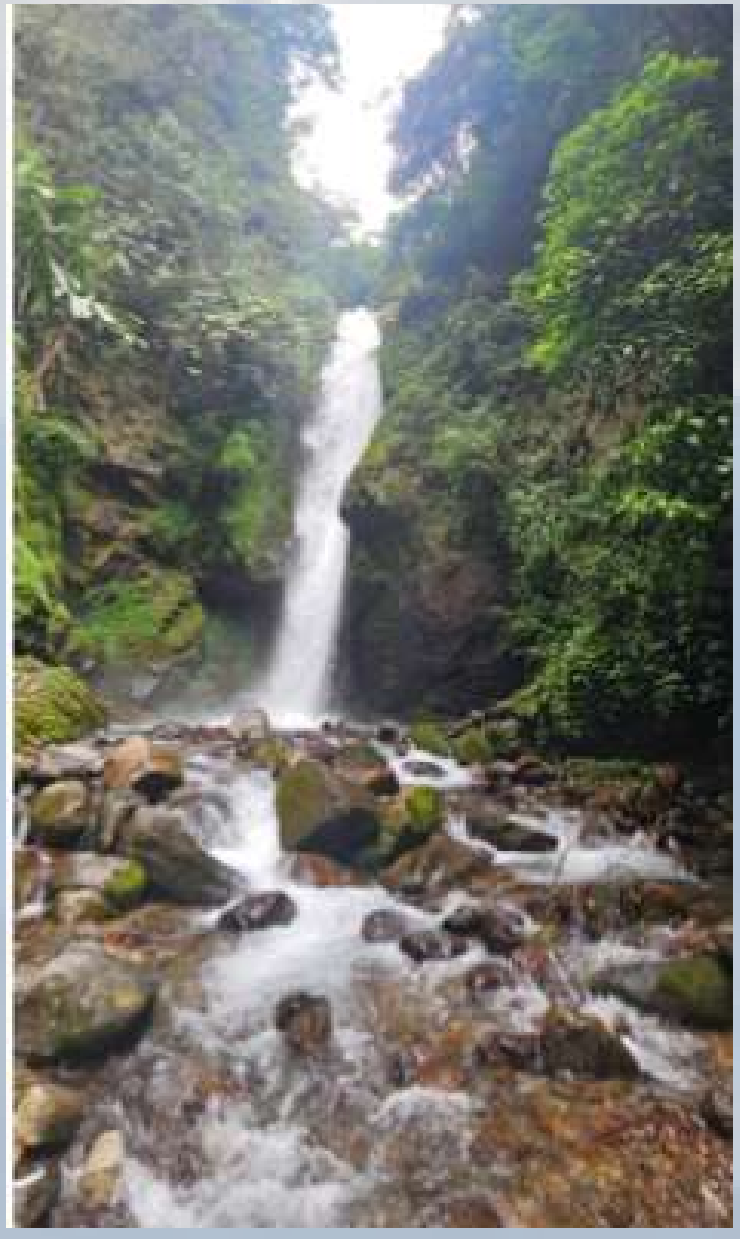
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